1.Overview of X7083/X7043/X7023

1-1 Introduction

X7083/X7043/X7023 is an LSI that generates a pulse for controlling the speed and positioning of pulse train input-type servo motors and stepping motors. X7083 enables 8-axis control, X7043 enables 4-axis control, X7023 enables 2-axis control.

This unit is comprised of an S-shaped or linear acceleration/deceleration pulse generator, a linear interpolation divider, an automatic deceleration point calculator based on trapezoidal or triangular drive, multi-counter and encoder inputs that can be used as the current position counter or deviation counter, a return-to-origin sensor interface, a limit sensor interface, a servo drive interface, an 8-bit general-purpose input, and an 8-bit general-purpose output.

Since X7083/X7043/X7023 provides an interface with a host CPU, it can be used as a peripheral LSI.

1-2 Features

◇ CPU interface

- ● Applicable microcomputers: 80 series, 68 series, etc.
- ● Address occupancy: 6 bits (64 bytes) for X7083, 5 bits (32 bytes) for X7043, and 4 bits (16 bytes) for X7023
- ● Data bit width: 8 bits

◇ Drive commands

- ● Index drive:
- ● Continuous pulse drive:
- ● Return-to-origin drive:
- ● Sensor positioning drive:

◇ Drive modes

- ● Acceleration/deceleration mode: S-shaped (sine, parabolic), linear
- ● Deceleration start point: Automatic calculation, manual setting, offset setting
- ● Synchronization mode: Multi-axis linear interpolation, sync start

◇ Encoder counter

- ● Number of counters: 2
- ● Bit length: 24 bits/32 bits switchable
- ● Count inputs: Internal pulse only, external-input pulses only, Internal pulse and external-input pulses

◇ Encoder converter inputs

- ● Number of channels: 1 channel
- ● Input format: 2-clock, 2-phase clock with 90º phase error
- ● Multiplication: 1/2/4 multiplication

◇ Comparator

- ● Bit length: 24 bits
- ● Comparison targets: Register and counter, counter and counter
- ● Comparison methods: ＝ , ＞
- ● Comparison output: 1 point (＝ or ＞), only for X7043 and X7023

◇ I/O

- ● Inputs: 8
- ● Outputs 8

◇ Other functions

- ● Independent setting functions for accelerator and decelerator
- ● Timer function
- ● Input filtering function
- ● Interrupt function
- ● I/O logic switching function
- ● Status functions

◇ Clock: 20.0 MHz（max.), 16.384 MHz or19.6608 MHz recommended

◇ Technology: CMOS

◇ Power source: Internal voltage: 3.3 V IO voltage: 5 V or 3.3 V

◇ Operating temperatures: 0 to +70 ℃

◇ Package: X7083 208-pin LQFP 28 x 28 (mm)

X7043 144-pin LQFP 20 x 20（mm）

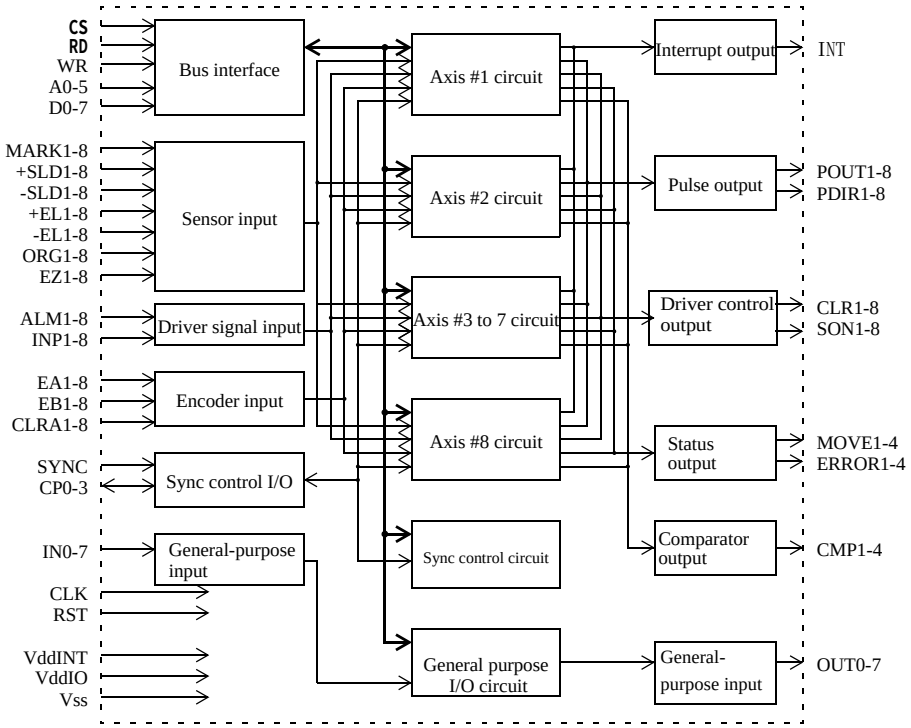
X7023 100-pin TQFP 14 x14（mm）

Lead-free specification: Sn-1 to 4Bi solder

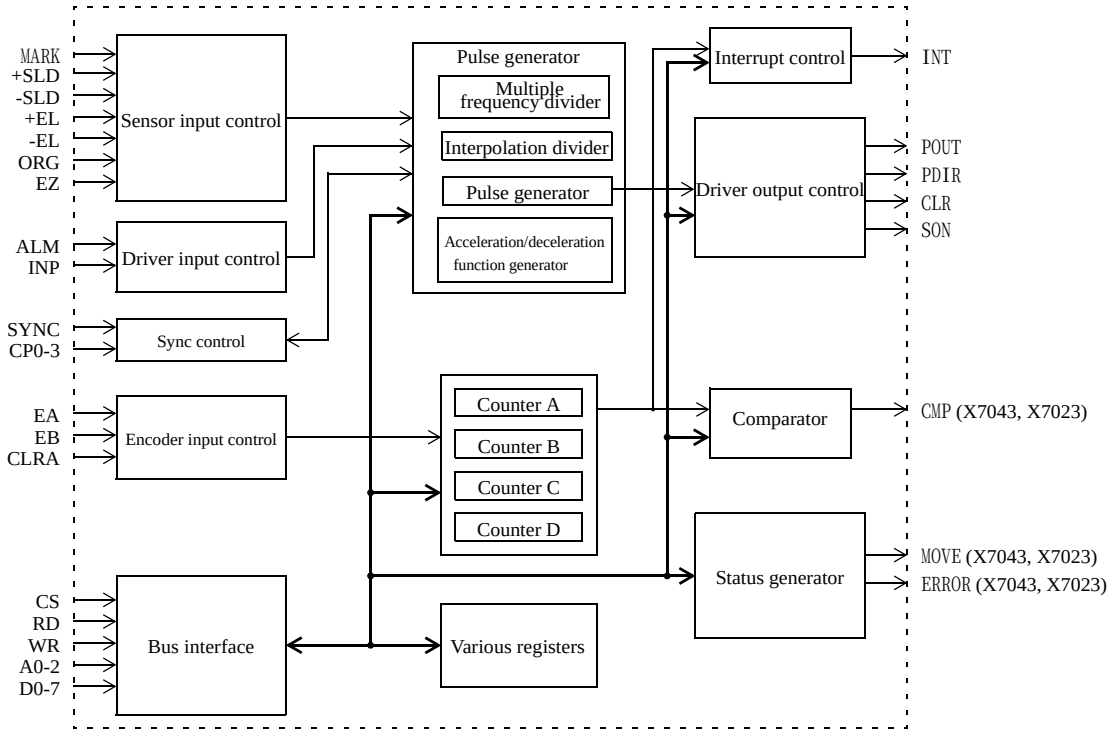
1-3 Block Diagram

Figure 1-1: Block Diagram

Overall Block Diagram and I/O Signals



Circuit Block Diagram for Axes #1 to #8



Only X7043 and X7023 have CP0-3, ERROR, and CMP.
X7083 has axes #1 to #8, X7043 axes #1 to #4, and X7023 axes #1 to #2.

1-4 Specifications List

Table 1-1: Specifications List

Item	Specifications
Supply voltage	Internal voltage 3.3 V ±10% I/O voltage 5 V ±10% or 3.3V ±5%
Input/output level	CMOS level
Max. input clock (f)	20.0 MHz (max), 16.384 MHz or 19.6608 MHz recommended
Max. output frequency	Linear acceleration/deceleration: 5 Mpps S-shaped acceleration/deceleration: 3.05 Mpps
Acceleration/deceleration time	Approx. 8 ms to 131 s (16382 steps, f = 16.384 MHz)
Output pulse count setting range (R_1)	1 to 16,777,215
Deceleration start point setting range (R_2)	0 to 16,777,215 (manual setting) -8388608 to 8388607 (auto-calculated offset setting)
Frequency multiplication ratio setting range (R_0)	1 to 4095
Frequency setting step count (R_3,R_4)	Linear acceleration/deceleration, S-shaped acceleration/deceleration and deceleration point manual setting mode: 1 to 16383 S-shaped acceleration/deceleration and deceleration start point automatic calculation mode: 1 to 10000
Acceleration/deceleration rate setting range (R_5,R_6)	1 to 16383
S-shaped section setting range (R_7)	1 to 8191
Sensor input sensitivity setting range (F)	0 to 255 Approx. 0.98 to 250 μs (f = 16.384 MHz)
Driver interface	Outputs: Clock output: Gate control/2-clock switchable, logic switchable 1-shot output: Approx. 1.9 μs (f = 16.384 MHz), logic switchable Servo ON output: General-purpose output Inputs: Driver alarm input: 1 point per axis, logic switchable Positioning end input: 1 point per axis, logic switchable
Sensor inputs	End limit inputs: 2 points, +/- directions, logic switchable Slow-down inputs: 2 points, +/- directions, logic switchable Slow-down/slow-down stop switchable Origin input: 2 points per axis, origin and Z phase, logic switchable Mark sensor input: 1 point per axis, logic switchable
General-purpose inputs/outputs	Inputs: 8 points Outputs: 8 points
Encoder interface	Input: One channel per axis, 2 clocks, 1/2/4 multiplication
Other inputs/outputs	Sync start input: 1 point Counter clear inputs: 1 point per axis Comparator output: 1 point per axis (only for X7043 and X7023)
Operating temperatures	0 to +70°C
Storage temperatures	-65 to +150°C
Dimensions	X7083 208PIN LQFP 28 x 28 (mm) X7043 144PIN LQFP 20 x 20 (mm) X7023 100PIN TQFP 14 x 14 (mm) Lead-free specification Sn-1 to 4Bi solder

1-5 Package Dimension Diagram

Figure 1-2: Package Dimension Diagram (X7083)

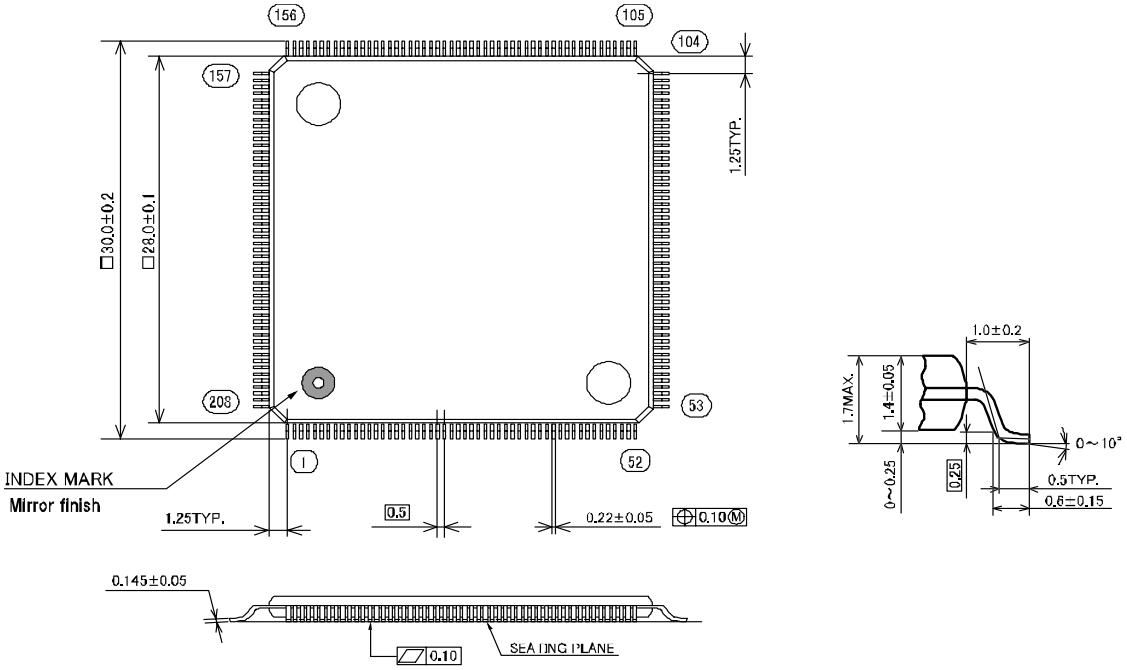


Figure 1-3: Package Dimension Diagram (X7043)

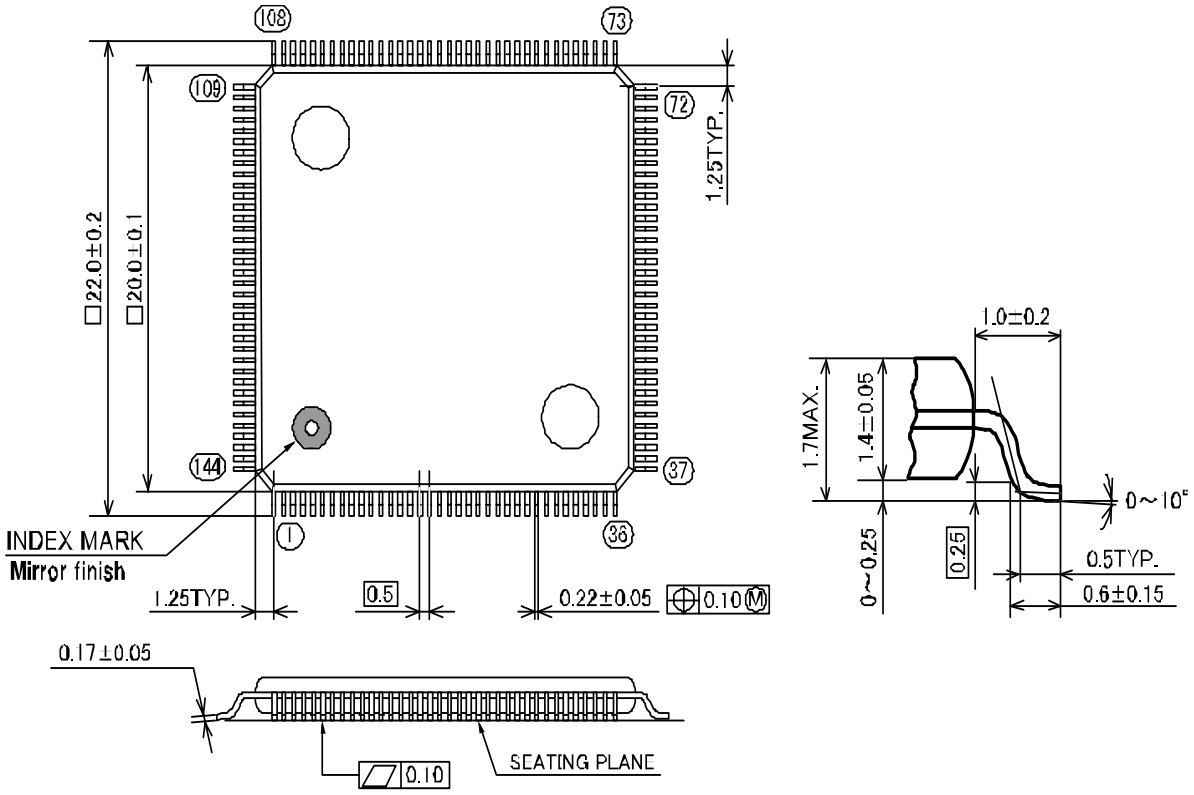
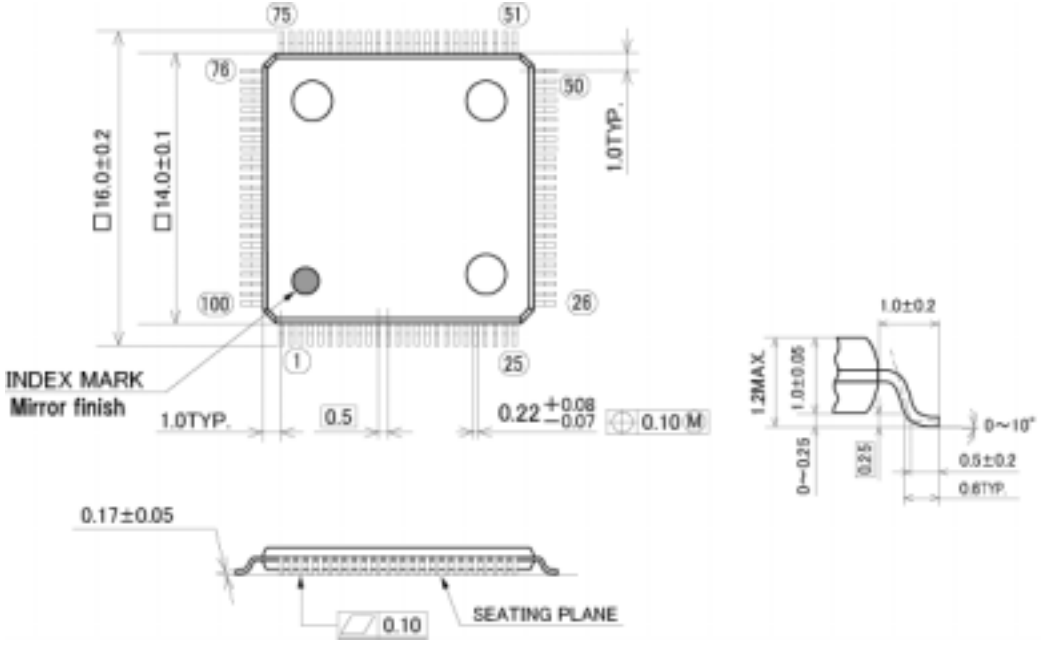


Figure 1-4: Package Dimension Diagram (X7023)



1-6 Pin Layout, Terminal Description

1-6-1 Terminal Description

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
26, 78, 130, 182	54, 126	37, 87	VddINT	—		+3.3 V ±10% power input.
8, 11, 17, 23, 37, 49, 55, 61, 72, 85, 100, 115, 134, 151, 168, 186, 203	7, 19, 46, 58, 79, 98, 117, 138	7, 18, 44, 54, 73, 94	VddIO	—		+5 V ±10% or 3.3V ±5% power input.
9, 12, 18, 24, 27, 38, 40, 50, 56, 62, 73, 79, 86, 101, 116, 131, 135, 152, 169, 183, 187, 204	9, 14, 21, 30, 47, 55, 59, 80, 99, 118, 127, 139	9, 20, 28, 38, 45, 55, 74, 88, 95	GND	—		0 V power input.
10	8	8	CLK	I	+	Reference clock input. Max. input frequency 20 MHz. Duty 50 ±10%
25	20	19	$\overline{RST}$	I	-	Rest signal. The LSI is reset when Low input of more than 3 reference clock periods is input.
34	27	25	$\overline{CS}$	I	-	Chip select signal. This LSI can be accessed when this pin goes Low.
35	28	26	$\overline{RD}$	I	-	Read enable signal. Data can be read out when $\overline{CS}$ is Low and $\overline{RD}$ is Low.
36	29	27	$\overline{WR}$	I	-	Write enable signal. Data can be loaded at the positive-going edge of $\overline{WR}$ from Low to High while $\overline{CS}$ is Low.
33	26	24	A0	I	+	6-bit address bus from A0 (LSB) to A5 (MSB).
32	25	23	A1			
31	24	22	A2			
30	23	21	A3			
29	22	-	A4			
28	-	-	A5			
22	18	17	D0	I/O	+	8-bit 2-directional data bus from D0 (LSB) to D7 (MSB) is used to transfer data between the LSI and host. The output buffer of these pins are tri-state buffers.
21	17	16	D1			
20	16	15	D2			
19	15	14	D3			
16	13	13	D4			
15	12	12	D5			
14	11	11	D6			
13	10	10	D7			

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
39	31	29	$\overline{\text{INT}}$	O	+-	Interrupt request signal, which goes active according to factors including the pulse output, counter, sensor and comparator. This pin goes Low or High impedance state. The $\overline{\text{INT}}$ output can be masked with the interrupt control register. The interrupt request can be canceled by wiring the interrupt flag reset command corresponding to each interrupt factor.
2	143	99	$\overline{\text{ALM1}}$	I	+-	Driver alarm emergency stop unit. The input logic can be switched with the input setting register. The input sensitivity can be set to between 16 and 4096 times the reference clock period by means of the input sensitivity setting register.
193	122	78	$\overline{\text{ALM2}}$			
174	103	-	$\overline{\text{ALM3}}$			
157	84	-	$\overline{\text{ALM4}}$			
140	-	-	$\overline{\text{ALM5}}$			
121	-	-	$\overline{\text{ALM6}}$			
104	-	-	$\overline{\text{ALM7}}$			
87	-	-	$\overline{\text{ALM8}}$			
205	136	92	$\overline{\text{+EL1}}$	I	+-	+direction immediate stop end limit input. The input logic can be switched with the input setting register. The input sensitivity can be set to between 16 and 4096 times the reference clock period by means of the input sensitivity setting register.
188	115	71	$\overline{\text{+EL2}}$			
167	96	-	$\overline{\text{+EL3}}$			
150	77	-	$\overline{\text{+EL4}}$			
133	-	-	$\overline{\text{+EL5}}$			
114	-	-	$\overline{\text{+EL6}}$			
97	-	-	$\overline{\text{+EL7}}$			
80	-	-	$\overline{\text{+EL8}}$			
202	135	91	$\overline{\text{-EL1}}$	I	+-	- direction immediate stop end limit input. The input logic can be switched with the input setting register. The input sensitivity can be set to between 16 and 4096 times the reference clock period by means of the input sensitivity setting register.
185	114	70	$\overline{\text{-EL2}}$			
166	95	-	$\overline{\text{-EL3}}$			
149	76	-	$\overline{\text{-EL4}}$			
132	-	-	$\overline{\text{-EL5}}$			
113	-	-	$\overline{\text{-EL6}}$			
96	-	-	$\overline{\text{-EL7}}$			
77	-	-	$\overline{\text{-EL8}}$			
201	134	90	$\overline{\text{+SLD1}}$	I	+-	+ direction slow-down limit input. Slow-down and slow-down stop can be switched with the input mode setting register. The input sensitivity can be set to between 16 and 4096 times the reference clock period by means of the input sensitivity setting register. Level or edge operation.
184	113	69	$\overline{\text{+SLD2}}$			
165	94	-	$\overline{\text{+SLD3}}$			
148	75	-	$\overline{\text{+SLD4}}$			
129	-	-	$\overline{\text{+SLD5}}$			
112	-	-	$\overline{\text{+SLD6}}$			
95	-	-	$\overline{\text{+SLD7}}$			
76	-	-	$\overline{\text{+SLD8}}$			

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
200	133	89	$\overline{\text{-SLD1}}$	I	+-	- direction slow-down limit input. Slow-down and slow-down stop can be switched with the input mode setting register. The input sensitivity can be set to between 16 and 4096 times the reference clock period by means of the input sensitivity setting register. Level or edge operation.
181	112	68	$\overline{\text{-SLD2}}$			
164	93	-	$\overline{\text{-SLD3}}$			
147	74	-	$\overline{\text{-SLD4}}$			
128	-	-	$\overline{\text{-SLD5}}$			
111	-	-	$\overline{\text{-SLD6}}$			
94	-	-	$\overline{\text{-SLD7}}$			
75	-	-	$\overline{\text{-SLD8}}$			
206	137	93	$\overline{\text{ORG1}}$	I	+-	Origin sensor input. With the return-to-coordinate-basic-origin drive, the return-to-origin operation is based on either the $\overline{\text{ORG}}$ input alone or the $\overline{\text{ORG}}$ and $\overline{\text{EZ}}$ (Encoder phase Z) inputs. The input sensitivity is 1 or 16 times the reference clock period.
189	116	72	$\overline{\text{ORG2}}$			
170	97	-	$\overline{\text{ORG3}}$			
153	78	-	$\overline{\text{ORG4}}$			
136	-	-	$\overline{\text{ORG5}}$			
117	-	-	$\overline{\text{ORG6}}$			
98	-	-	$\overline{\text{ORG7}}$			
81	-	-	$\overline{\text{ORG8}}$			
207	140	96	$\overline{\text{EZ1}}$	I	+-	Encoder phase Z input. With the return-to-origin operation using the $\overline{\text{ORG}}$ and $\overline{\text{EZ}}$ inputs according to the return-to-coordinate-basic-origin drive, the operation stops when the $\overline{\text{EZ}}$ input is activated after deceleration, started by $\overline{\text{ORG}}$ going active, has completed. The input sensitivity is an edge operation based on sampling at the reference clock period.
190	119	75	$\overline{\text{EZ2}}$			
171	100	-	$\overline{\text{EZ3}}$			
154	81	-	$\overline{\text{EZ4}}$			
137	-	-	$\overline{\text{EZ5}}$			
118	-	-	$\overline{\text{EZ6}}$			
99	-	-	$\overline{\text{EZ7}}$			
82	-	-	$\overline{\text{EZ8}}$			
3	144	100	$\overline{\text{INP1}}$	I	+-	Servo driver positioning completion input. If the initial setting register has been set to turn the stop flag ON at the completion of positioning, the operation completion flag is set ON when the $\overline{\text{INP}}$ input becomes active after the completion of the pulse output. In case of normal stop interrupt, the $\overline{\text{INT}}$ output becomes activate similarly.
194	123	79	$\overline{\text{INP2}}$			
175	104	-	$\overline{\text{INP3}}$			
158	85	-	$\overline{\text{INP4}}$			
141	-	-	$\overline{\text{INP5}}$			
122	-	-	$\overline{\text{INP6}}$			
105	-	-	$\overline{\text{INP7}}$			
88	-	-	$\overline{\text{INP8}}$			
199	132	86	$\overline{\text{MARK1}}$	I	+-	Sensor positioning start input. When the sensor positioning drive is used, the set number of pulses are output when the $\overline{\text{MARK}}$ input becomes active. The input sensitivity is 1 or 16 times the reference clock period.
180	111	67	$\overline{\text{MARK2}}$			
163	92	-	$\overline{\text{MARK3}}$			
146	73	-	$\overline{\text{MARK4}}$			
127	-	-	$\overline{\text{MARK5}}$			
110	-	-	$\overline{\text{MARK6}}$			
93	-	-	$\overline{\text{MARK7}}$			
74	-	-	$\overline{\text{MARK8}}$			

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
48	45	43	$\overline{IN0}$	I	-	$\overline{IN0}$ (LSB) to $\overline{IN7}$ (MSB) form an 8-bit parallel input. Interrupt is possible at the change of $\overline{IN0}$ from High to Low.
47	44	42	$\overline{IN1}$			
46	43	41	$\overline{IN2}$			
45	42	40	$\overline{IN3}$			
44	41	39	$\overline{IN4}$			
43	40	36	$\overline{IN5}$			
42	39	35	$\overline{IN6}$			
41	38	34	$\overline{IN7}$			
71	64	58	$\overline{CLRA1}$	I	-	Multi-counter A is cleared to 0 when $\overline{CLRA}$ is Low. The level and edge operations can be switched.
70	63	57	$\overline{CLRA2}$			
69	62	-	$\overline{CLRA3}$			
68	61	-	$\overline{CLRA4}$			
67	-	-	$\overline{CLRA5}$			
66	-	-	$\overline{CLRA6}$			
65	-	-	$\overline{CLRA7}$			
64	-	-	$\overline{CLRA8}$			
7	4	4	$\overline{POUT1}$	O	+-	Instruction pulse output. Outputs the CW pulse when the 2-pulse method is used or outputs the pulse output when the pulse/direction method is used. The output logic can be switched with the output logic register.
198	129	83	$\overline{POUT2}$			
179	108	-	$\overline{POUT3}$			
162	89	-	$\overline{POUT4}$			
145	-	-	$\overline{POUT5}$			
126	-	-	$\overline{POUT6}$			
109	-	-	$\overline{POUT7}$			
92	-	-	$\overline{POUT8}$			
6	3	3	$\overline{PDIR1}$	O	+-	Direction output or instruction pulse output. Outputs the CCW pulse when the 2-pulse method is used or outputs the direction output when the pulse/direction method is used. The output logic can be switched with the output logic register.
197	128	82	$\overline{PDIR2}$			
178	107	-	$\overline{PDIR3}$			
161	88	-	$\overline{PDIR4}$			
144	-	-	$\overline{PDIR5}$			
125	-	-	$\overline{PDIR6}$			
108	-	-	$\overline{PDIR7}$			
91	-	-	$\overline{PDIR8}$			
4	1	1	$\overline{CLR1}$	O	+-	1-shot or general-purpose output for clearing the deviation counter of the servo driver. The 1-shot and general-purpose outputs can be switched with the initial setting register of the output. The pulse duration of shot is 32 times the reference clock period. The output logic can be switched with the output logic register.
195	124	80	$\overline{CLR2}$			
176	105	-	$\overline{CLR3}$			
159	86	-	$\overline{CLR4}$			
142	-	-	$\overline{CLR5}$			
123	-	-	$\overline{CLR6}$			
106	-	-	$\overline{CLR7}$			
89	-	-	$\overline{CLR8}$			

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
5	2	2	$\overline{\text{SON1}}$	O	-	Servo ON output for the servo driver. Can be used as the general-purpose output
196	125	81	$\overline{\text{SON2}}$			
177	106	-	$\overline{\text{SON3}}$			
160	87	-	$\overline{\text{SON4}}$			
143	-	-	$\overline{\text{SON5}}$			
124	-	-	$\overline{\text{SON6}}$			
107	-	-	$\overline{\text{SON7}}$			
90	-	-	$\overline{\text{SON8}}$			
60	57	53	$\overline{\text{OUT0}}$	O	-	$\overline{\text{OUT0}}$ (LSB) to $\overline{\text{OUT7}}$ (MSB) form an 8-bit parallel, general-purpose output. The 8 bits can be rewritten simultaneously while the bit operation of each bit is possible.
59	56	52	$\overline{\text{OUT1}}$			
58	53	51	$\overline{\text{OUT2}}$			
57	52	50	$\overline{\text{OUT3}}$			
54	51	49	$\overline{\text{OUT4}}$			
53	50	48	$\overline{\text{OUT5}}$			
52	49	47	$\overline{\text{OUT6}}$			
51	48	46	$\overline{\text{OUT7}}$			
-	6	6	$\overline{\text{ERROR1}}$	O	+-	Error stop monitoring output. Goes Low in case of error stop due to $\overline{\text{ALM}}$, $\overline{\text{+EL}}$ and $\overline{\text{-EL}}$. Goes High when the stop flag is reset. The output logic can be switched with the output logic register. This function is not available for X7083.
	131	85	$\overline{\text{ERROR2}}$			
	110	-	$\overline{\text{ERROR3}}$			
	91	-	$\overline{\text{ERROR4}}$			
-	5	5	$\overline{\text{MOVE1}}$	O	+-	Monitoring output in the pulse output. Goes Low while pulses are output. The output logic can be switched with the output logic register. This function is not available for X7083.
	130	84	$\overline{\text{MOVE2}}$			
	109	-	$\overline{\text{MOVE3}}$			
	90	-	$\overline{\text{MOVE4}}$			
1	142	98	$\overline{\text{EA1}}$	I	-	Phase A input of encoder input. The 2-clock method and the 1/2/4 multiplication of the 90 ^{o} phase difference can be selected with the initial setup of the encoder input/output.
192	121	77	$\overline{\text{EA2}}$			
173	102	-	$\overline{\text{EA3}}$			
156	83	-	$\overline{\text{EA4}}$			
139	-	-	$\overline{\text{EA5}}$			
120	-	-	$\overline{\text{EA6}}$			
103	-	-	$\overline{\text{EA7}}$			
84	-	-	$\overline{\text{EA8}}$			

Table 1-2: Terminal Description

Terminal No. X7083	Terminal No. X7043	Terminal No. X7023	Signal	I/O	Logic	Description
208 191 172 155 138 119 102 83	141 120 101 82 - - - -	97 76 - - - - - -	$\overline{EB1}$ $\overline{EB2}$ $\overline{EB3}$ $\overline{EB4}$ $\overline{EB5}$ $\overline{EB6}$ $\overline{EB7}$ $\overline{EB8}$	I	-	Phase B input of encoder input. The 2-clock method and the 1/2/4 multiplication of the 90° phase difference can be selected with the initial setup of the encoder input/output.
-	37 36 35 34	33 32 - -	$\overline{CMP1}$ $\overline{CMP2}$ $\overline{CMP3}$ $\overline{CMP4}$	O	-	Comparison output between a comparator register and counter (A, B or C) or between counters. = and > can be switched with the comparator control register. This function is not available for X7083.
63	60	56	$\overline{SYNC}$	I	-	Sync start input. When the sync start mode is activated, the pulse starts to be output when $\overline{SYNC}$ changes from High to Low.
-	72 71 70 69	66 65 64 63	$\overline{CP0}$ $\overline{CP1}$ $\overline{CP2}$ $\overline{CP3}$	I/O	-	Linear interpolation status inputs/outputs. When linear interpolation is performed by using several units of the LSI, connect $\overline{CP0}$, $\overline{CP1}$, $\overline{CP2}$ and $\overline{CR3}$ of the LSIs respectively with wired OR. The output buffer is an open-drain buffer. The functions of the terminals are listed below. Priority: 1 $\overline{CP0}$ Immediate stop; 2 $\overline{CP1}$ Deceleration/stop; 3 $\overline{CP2}$ Constant speed; 4 $\overline{CP3}$ Deceleration This terminal is not available for X7083.
-	32,33,65, 66,67,68	30,31,59, 60,61,62	NC			No connection.

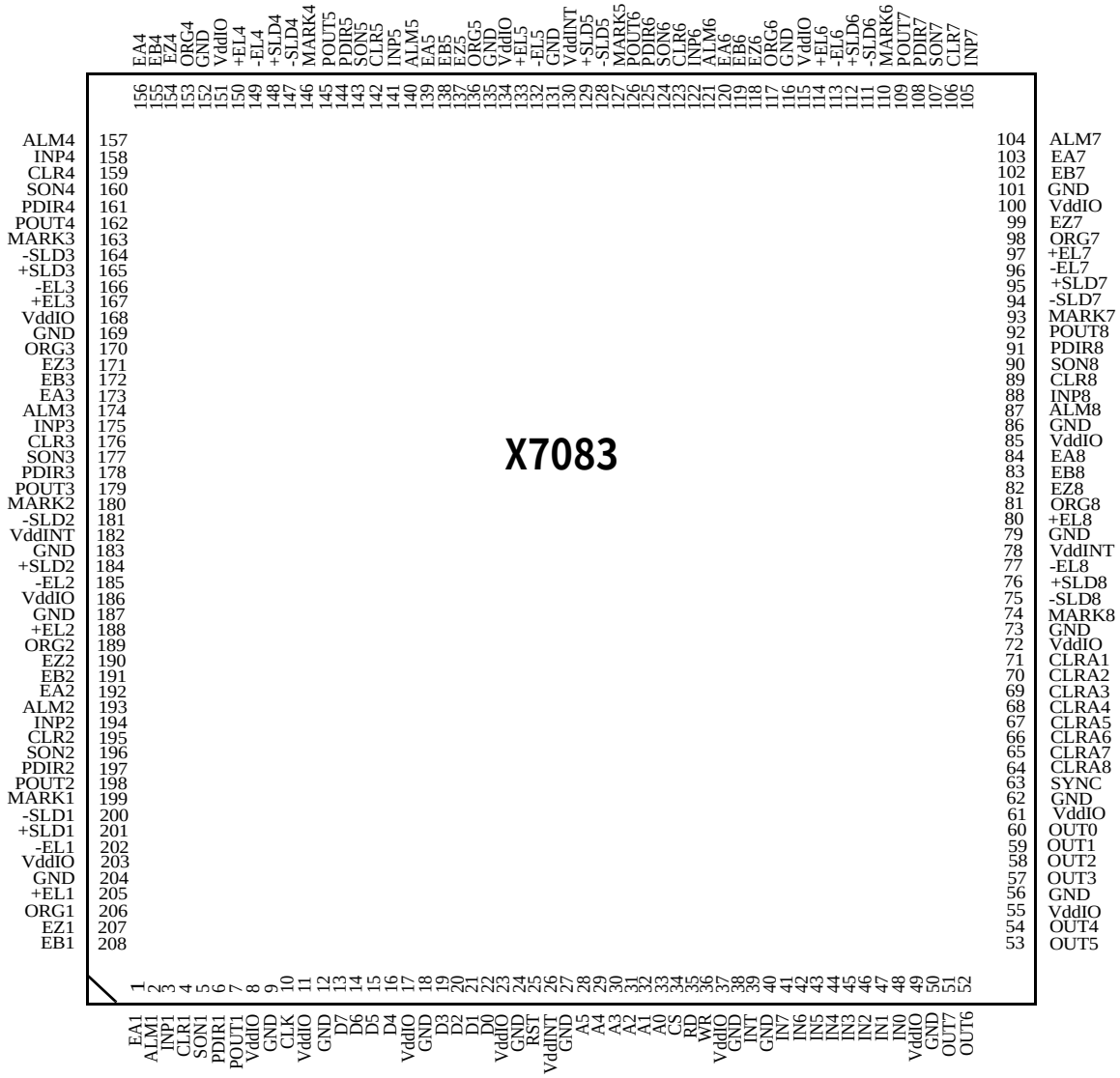
[Note] 1. $\overline{INT}$ is an open drain output.

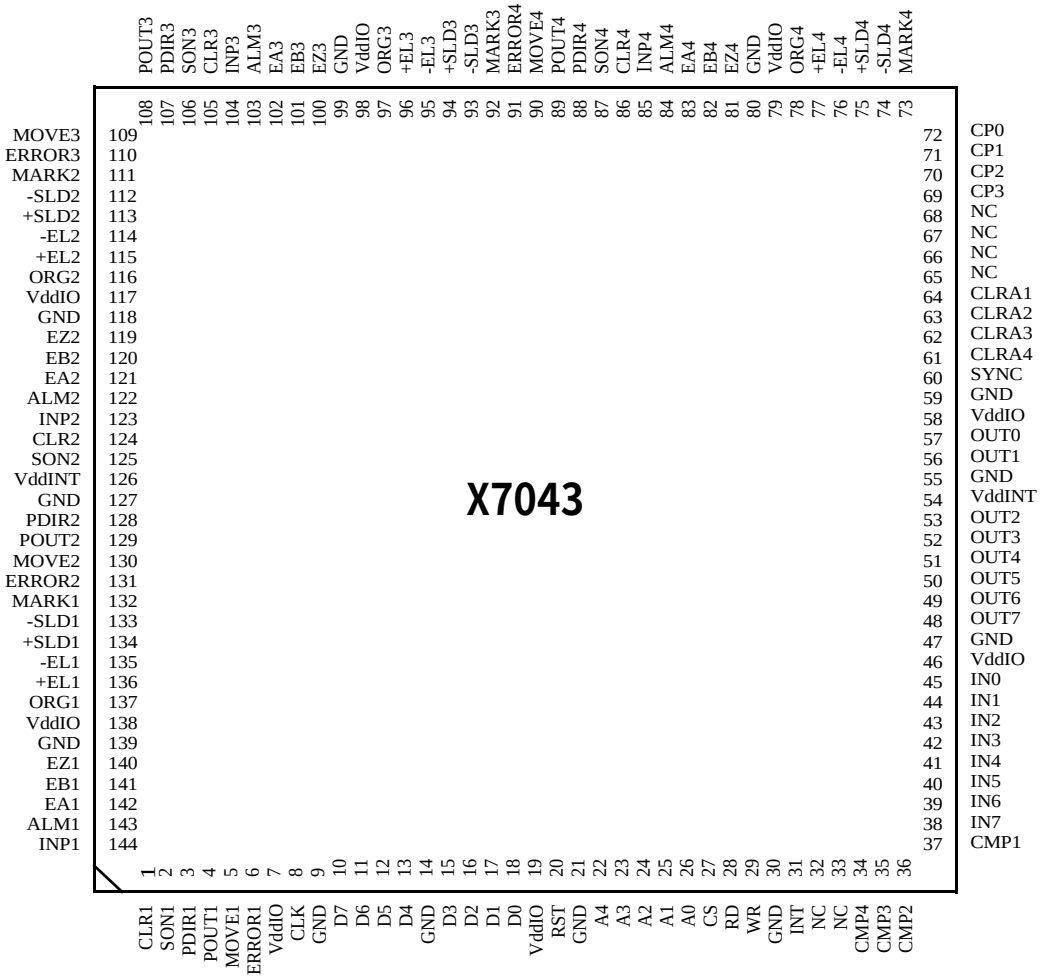
2. $\overline{ALM}$, $\overline{+EL}$, $\overline{-EL}$, $\overline{+SLD}$, $\overline{-SLD}$, $\overline{ORG}$, $\overline{EZ}$, $\overline{INP}$, $\overline{MARK}$, $\overline{IN0\text{-}7}$, $\overline{EA}$, $\overline{EB}$, $\overline{SYNC}$, and $\overline{CLRA}$ are inputs with built-in pull-up resistance (75kΩ).

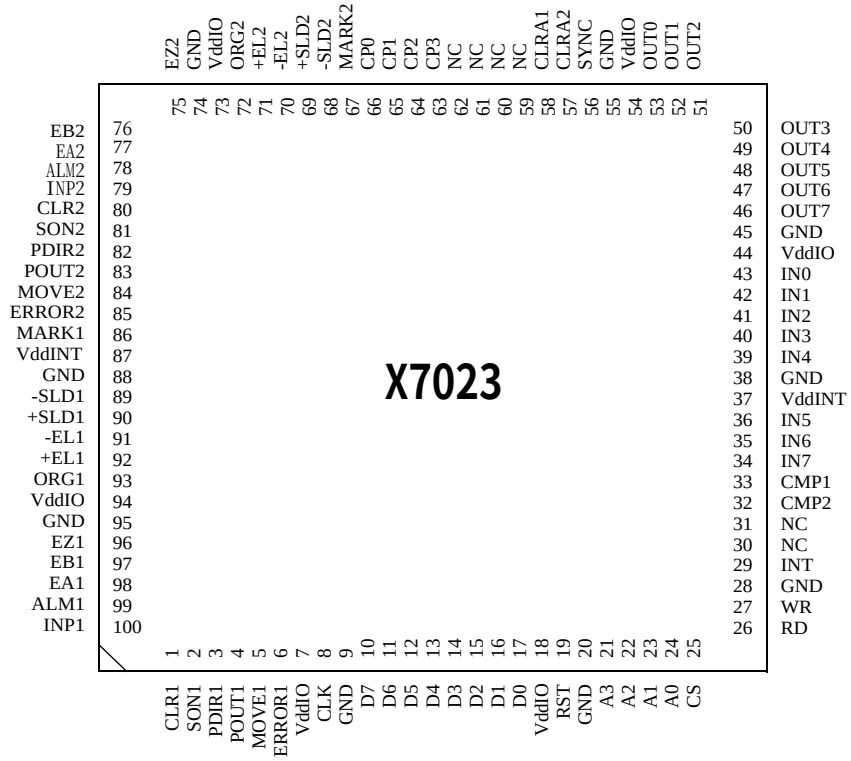
3. $\overline{CP0\text{-}3}$ is an input/output with built-in pull-up resistance (75kΩ).

1-6-2 Pin Lay-out

Figure 1-5:Pin Lay-out




X7043
1 CLR1
2 SON1
3 PDIR1
4 POUT1
5 MOVE1
6 ERROR1
7 VddIO
8 CLK
9 GND
10 D7
11 D6
12 D5
13 D4
14 GND
15 D3
16 D2
17 D1
18 D0
19 VddIO
20 RST
21 GND
22 A4
23 A3
24 A2
25 A1
26 A0
27 CS
28 RD
29 WR
30 GND
31 INT
32 NC
33 NC
34 CMP4
35 CMP3
36 CMP2
37 CMP1
38 IN7
39 IN6
40 IN5
41 IN4
42 IN3
43 IN2
44 IN1
45 IN0
46 VddIO
47 GND
48 OUT7
49 OUT6
50 OUT5
51 OUT4
52 OUT3
53 OUT2
54 VddINT
55 GND
56 OUT1
57 OUT0
58 VddIO
59 GND
60 SYNC
61 CLRA4
62 CLRA3
63 CLRA2
64 CLRA1
65 NC
66 NC
67 NC
68 NC
69 CP3
70 CP2
71 CP1
72 CP0
73 MARK4
74 SLD4
75 SLD4
76 EL4
77 EL4
78 ORG4
79 VddIO
80 GND
81 EZ4
82 EB4
83 EA4
84 ALM4
85 INP4
86 CLR4
87 SON4
88 PDIR4
89 POUT4
90 MOVE4
91 ERROR4
92 MARK3
93 SLD3
94 SLD3
95 EL3
96 EL3
97 ORG3
98 VddIO
99 GND
100 EZ3
101 EB3
102 EA3
103 ALM3
104 INP3
105 CLR3
106 SON3
107 PDIR3
108 POUT3
109 MOVE3
110 ERROR3
111 MARK2
112 SLD2
113 SLD2
114 EL2
115 EL2
116 ORG2
117 VddIO
118 GND
119 EZ2
120 EB2
121 EA2
122 ALM2
123 INP2
124 CLR2
125 SON2
126 VddINT
127 GND
128 PDIR2
129 POUT2
130 MOVE2
131 ERROR2
132 MARK1
133 SLD1
134 SLD1
135 EL1
136 EL1
137 ORG1
138 VddIO
139 GND
140 EZ1
141 EB1
142 EA1
143 ALM1
144 INP1


X7023
1 CLR1
2 SON1
3 PDIR1
4 POUT1
5 MOVE1
6 ERROR1
7 VddIO
8 CLK
9 GND
10 D7
11 D6
12 D5
13 D4
14 D3
15 D2
16 D1
17 D0
18 VddIO
19 RST
20 GND
21 A3
22 A2
23 A1
24 A0
25 CS
26 RD
27 WR
28 GND
29 INT
30 NC
31 NC
32 CMP2
33 CMP1
34 IN7
35 IN6
36 IN5
37 VddINT
38 GND
39 IN4
40 IN3
41 IN2
42 IN1
43 IN0
44 VddIO
45 GND
46 OUT7
47 OUT6
48 OUT5
49 OUT4
50 OUT3
51 OUT2
52 OUT1
53 OUT0
54 VddIO
55 GND
56 SYNC
57 CLRA2
58 CLRA1
59 NC
60 NC
61 NC
62 NC
63 CP3
64 CP2
65 CP1
66 CP0
67 MARK2
68 SLD2
69 SLD2
70 EL2
71 EL2
72 ORG2
73 VddIO
74 GND
75 EZ2
76 EB2
77 EA2
78 ALM2
79 INP2
80 CLR2
81 SON2
82 PDIR2
83 POUT2
84 MOVE2
85 ERROR2
86 MARK1
87 VddINT
88 GND
89 SLD1
90 SLD1
91 EL1
92 EL1
93 ORG1
94 VddIO
95 GND
96 EZ1
97 EB1
98 EA1
99 ALM1
100 INP1

1-7 System Configuration

Figure 1-6: Example of a Servo Motor Interface

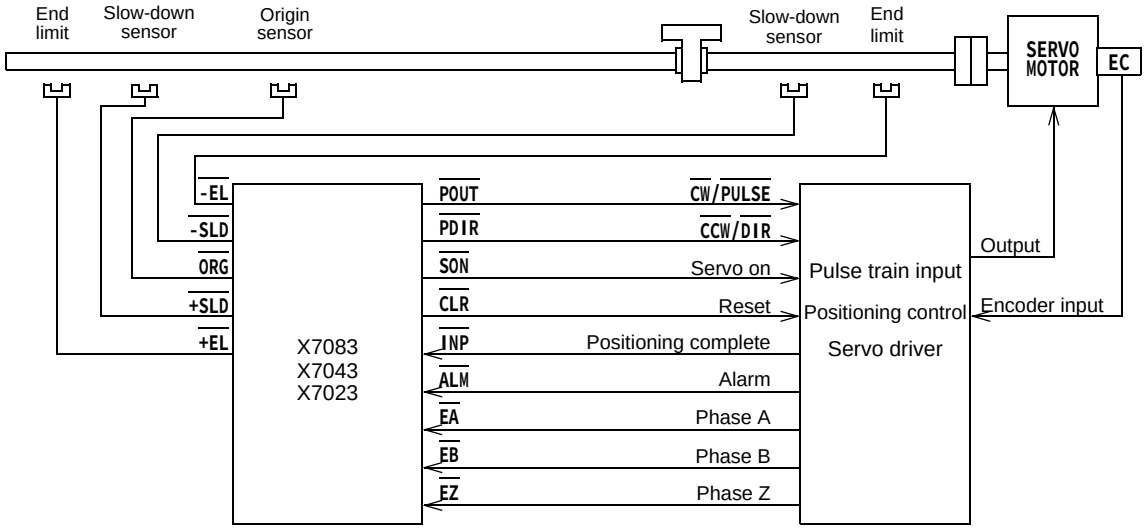
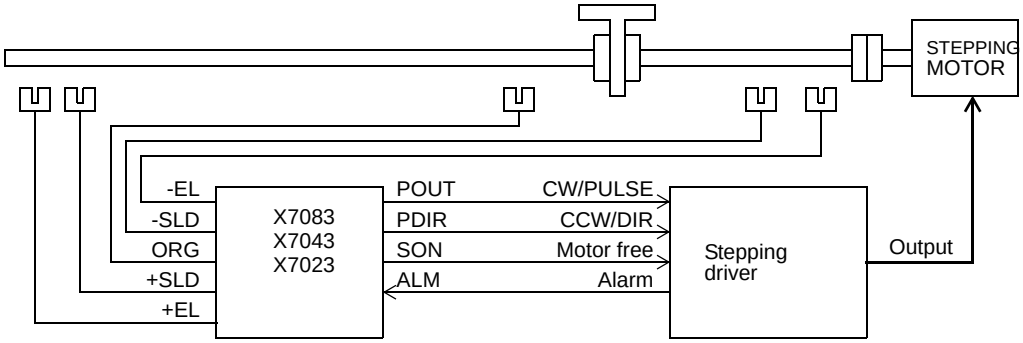


Figure 1-7: Example of a Stepping Motor Interface

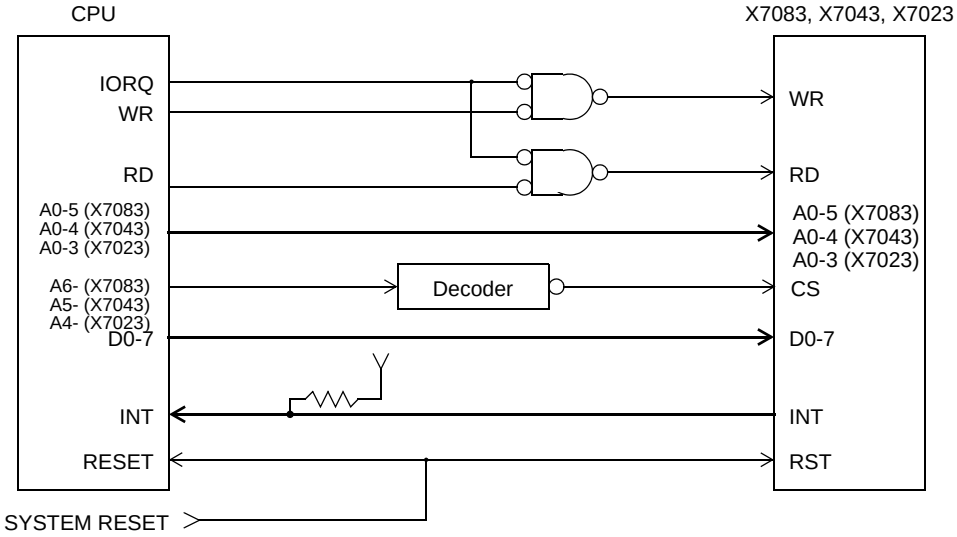


1-8 Example of Interfacing with CPU

This LSI uses a bus interface which can be connected to a 80-series processor through the 8-bit data bus from D0 to D7. However, the LSI can also be interfaced with a 68-series processor providing a simple external circuit.

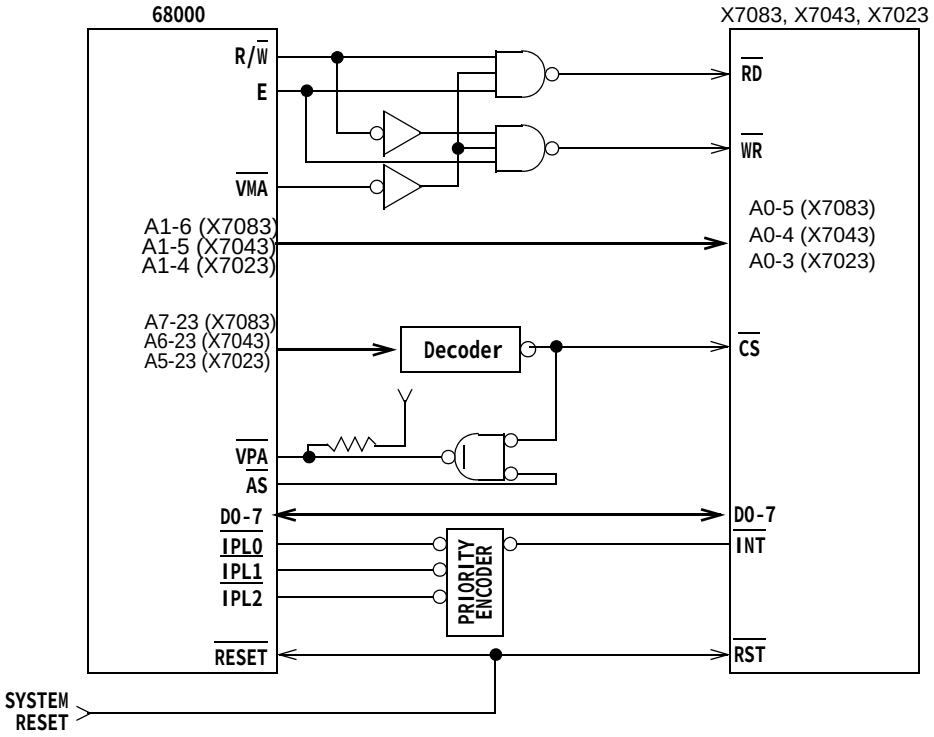
1-8-1 Example of Interfacing with Z80

Figure 1-8: Example of Interfacing with Z80



1-8-2 Example of Interfacing with 68000

Figure 1-9: Example of Interfacing with 68000



2. Address Allocation and Data Read/Write

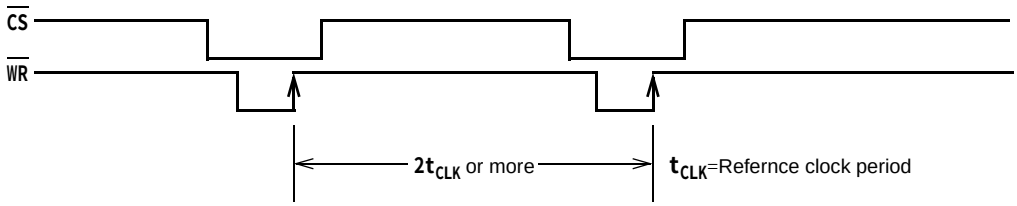
2-1 Address Allocation

Table 2-1: Address Allocation Table

A5	A4	A3	A2	A1	A0	Write	Read
0	0	0	0	0	0	Axis #1 register selector	Axis #1 register selector
0	0	0	0	0	1	Axis #1 write data 1 (bit0-7)	Axis #1 read data 1 (bit0-7)
0	0	0	0	1	0	Axis #1 write data 2 (bit8-15)	Axis #1 read data 2 (bit8-15)
0	0	0	0	1	1	Axis #1 write data 3 (bit16-23)	Axis #1 read data 3 (bit16-23)
0	0	0	1	0	0	Axis #1 write data 4 (bit24-31)	Axis #1 read data 4 (bit24-31)
0	0	0	1	0	1	Reserved by system (access prohibited)	Interrupt axis status
0	0	0	1	1	0	Reserved by system (access prohibited)	Axis #1 interrupt state status
0	0	0	1	1	1	Axis #1 command	Axis #1 operation state status
0	0	1	000b to 111b			Axis #2 access area Same allocation as axis #1	
0	1	0	000b to 111b			Axis #3 access area Same allocation as axis #1	
0	1	1	000b to 111b			Axis #4 access area Same allocation as axis #1	
1	0	0	000b ～ 111b			Axis #5 access area Same allocation as axis #1	
1	0	1	000b ～ 111b			Axis #6 access area Same allocation as axis #1	
1	1	0	000b ～ 111b			Axis #7 access area Same allocation as axis #1	
1	1	1	000b ～ 111b			Axis #8 access area Same allocation as axis #1	

[Note] 1. The Write cycles require the time of 2 reference clock periods (recovery time) to write data.

Figure 2-1: Write Cycle and Recovery Time



2. Parameters other than the command write, interrupt status monitoring and operation status monitoring parameters, and the counter initial setting can be read or written in Write data 1 to 4 or Read data 1 to 4 after the register selector has been set.
3. When an item of Write data is 2 bytes or more, the write operation begins with the lowest data and goes on toward the higher data. The data is written simultaneously when the highest byte has been written.
4. When an item of read data is 2 bytes or more, it is read after writing the register selector. The data is latched in the auxiliary buffer for simultaneous read at the moment the register selector is written. The read operation is performed continuously.

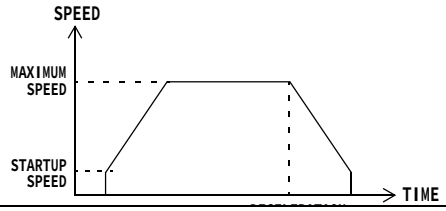
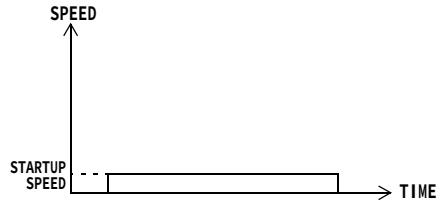
3. Command Types and Functions

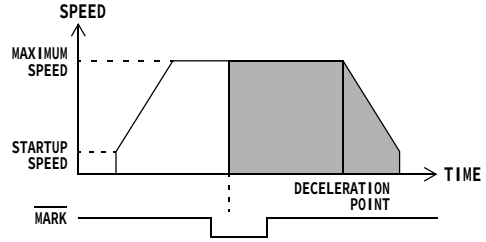
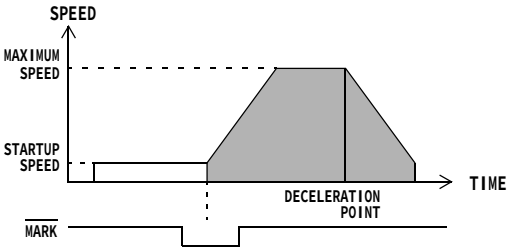
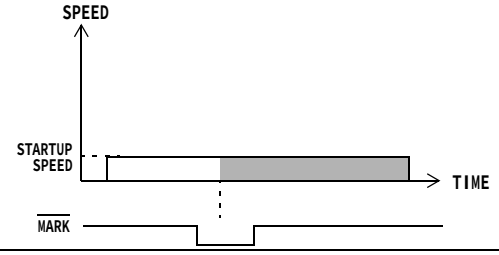
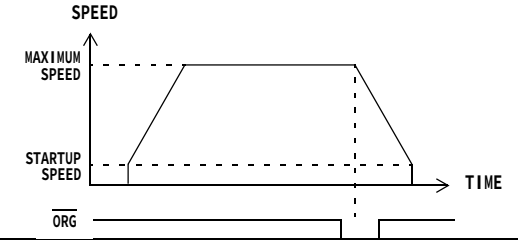
3-1 Command Write

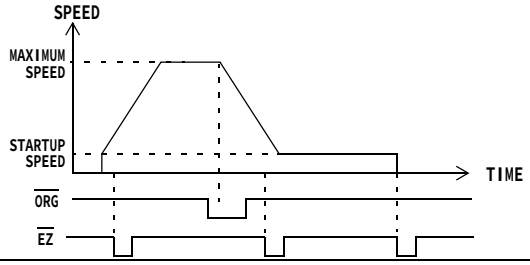
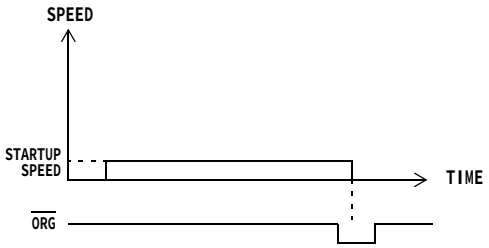
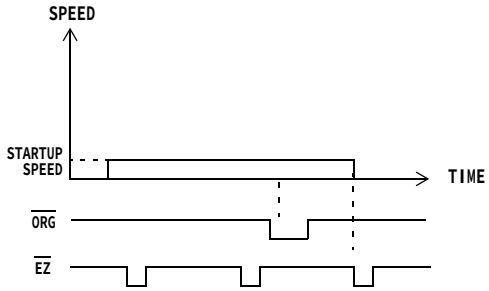
Writes a 1-byte command code to the command register.

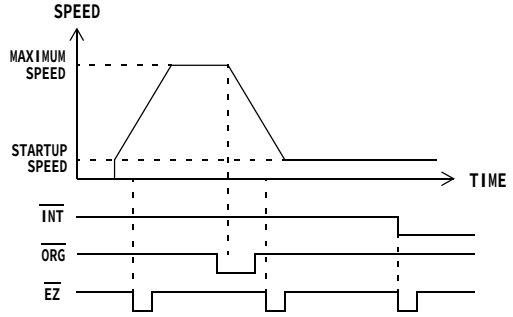
3-2 Command List

Table 3-1: Command List

Command code (hex)	Type	Description
00h	Index drive (+ direction)	Positioning drive accompanied with acceleration and deceleration. 
01h	Index drive (- direction)	
02h	Constant-speed index drive (+ direction)	Positioning drive at the startup speed. 
03h	Constant-speed index drive (- direction)	
06h	Continuous drive (+ direction)	Continuous pulse drive accompanied with acceleration. The pulse is output until the immediate stop command (command 30h) or deceleration stop command (command 31h) is written or until $\overline{+EL}$, $\overline{-EL}$ or $\overline{ALM}$ goes active.
07h	Continuous drive (- direction)	
08h	Constant-speed continuous drive (+ direction)	Continuous pulse drive at the start up speed. The pulse is output until the immediate stop command (command 30h) or deceleration stop command (command 31h) is written or until $\overline{+EL}$, $\overline{-EL}$ or $\overline{ALM}$ goes active.
09h	Constant-speed continuous drive (- direction)	

Command code (hex)	Type	Description
0Ah	Sensor positioning drive I (+ direction)	Positioning drive from the position where the $\overline{\text{MARK}}$ input terminal goes active. Acceleration starts from the beginning of the drive. 
0Bh	Sensor positioning drive I (- direction)	
0Ch	Sensor positioning drive II (+ direction)	Positioning drive from the position where the MARK input terminal goes active. Acceleration starts when the $\overline{\text{MARK}}$ input goes active. 
0Dh	Sensor positioning drive II (- direction)	
0Eh	Sensor positioning drive III (+ direction)	Positioning drive from the position where the $\overline{\text{MARK}}$ input terminal goes active. Acceleration and deceleration are not performed. 
0Fh	Sensor positioning drive III (- direction)	
12h	Return-to-origin I (+ direction)	Return-to-origin accompanied with acceleration and deceleration. The drive decelerates and stops when $\overline{\text{ORG}}$ goes active. 
13h	Return-to-origin I (- direction)	

<table>
<tr><th>Command code (hex)</th><th>Type</th><th>Description</th></tr>
<tr><td>14h</td><td>Return-to-origin II (+ direction)</td><td rowspan="2">Return-to-origin accompanied with acceleration and deceleration. The drive decelerates when $\overline{\text{ORG}}$ goes active and stops when $\overline{\text{EZ}}$ goes active after reaching startup speed.
 
</td></tr>
<tr><td>15h</td><td>Return-to-origin II (- direction)</td></tr>
<tr><td>16h</td><td>Return-to-origin III (+ direction)</td><td rowspan="2">Return-to-origin at the startup speed. Immediate stop occurs when $\overline{\text{ORG}}$ goes active.
 
</td></tr>
<tr><td>17h</td><td>Return-to-origin III (- direction)</td></tr>
<tr><td>18h</td><td>Return-to-origin IV (+ direction)</td><td rowspan="2">Return-to-origin at the startup speed. Immediate stop occurs when $\overline{\text{EZ}}$ goes active after $\overline{\text{ORG}}$ has been activated.
 
</td></tr>
<tr><td>19h</td><td>Return-to-origin IV (- direction)</td></tr>
</table>

Command code (hex)	Type	Description
1Ah	Return-to-origin V (+ direction)	Return-to-origin accompanied with acceleration and deceleration. When $\overline{\text{ORG}}$ goes active, deceleration occurs and the interrupt with the $\overline{\text{EZ}}$ input is enabled. When the return-to-origin II command is executed, stops at the next edge where $\overline{\text{EZ}}$ goes active. 
1Bh	Return-to-origin V (- direction)	
30h	Immediate stop command	Immediate stop occurs when this command is written during drive. However, the pulse duration of the last pulse is assured. In interpolation mode, only one axis stops.
31h	Deceleration stop command	The drive decelerates and stops when this command is written during drive. Immediate stop occurs if this command is written during constant speed drive. However, the pulse duration of the last pulse is assured. In interpolation mode, other axes also decelerate and stop.
32h	Deceleration command	The drive decelerates to the startup speed when this command is written during a drive accompanied with acceleration and deceleration. In interpolation mode, other axes also decelerate.
33h	Deceleration cancel command	The drive accelerates to the maximum speed when this command is written after the deceleration command. In interpolation mode, the deceleration of other axes is also canceled.
34h	Constant-speed command	The drive is fixed at the current speed when this command is written during a drive accompanied with acceleration and deceleration. In interpolation mode, the speed of other axes is also fixed at the current speed.
35h	Constant-speed cancel command	Acceleration/deceleration operation starts again when this command is written during the constant-speed drive command or after the constant-speed command. In interpolation mode, acceleration/deceleration operation starts again simultaneously for other axes too.
36h	Simultaneous stop command	All axes stop simultaneously when this command is written in interpolation mode.
40h	Timer operation I	Index drive without pulse output.
41h	Timer operation II	Constant-speed index drive without pulse output.

Command code (hex)	Type	Description
50h	Counter A clear command	Clears counter A to 0.
51h	Counter B clear command	Clears counter B to 0
A0h	Operation completion flag reset command	The operation completion flag is reset when this command is written while the flag is set. When the operation completion flag and error flag are set, this command resets both of them. As the operation cannot be restarted by writing a drive command while the operation completion flag is set, the flag must be reset using this command before writing a drive command.
A2h	Deceleration start interrupt flag reset command	The deceleration start interrupt flag is reset when this command is written while the flag is set.
A3h	ISO-speed interrupt flag reset command	The ISO-speed interrupt flag is reset when this command is written while the flag is set.
A5h	Maximum acceleration interrupt flag reset command	The maximum acceleration interrupt flag is reset when this command is written while the flag is set.
A8h	Counter A carry interrupt flag reset	The counter A carry interrupt flag will be reset if this command is written while the flag is set.
A9h	Counter A borrow interrupt flag reset	The counter A borrow interrupt flag will be reset if this command is written while the flag is set.
AAh	Counter B carry interrupt flag reset	The counter B carry interrupt flag will be reset if this command is written while the flag is set.
ABh	Counter B borrow interrupt flag reset	The counter B borrow interrupt flag will be reset if this command is written while the flag is set.
ADh	Counter C borrow interrupt flag reset	The counter C borrow interrupt flag will be reset if this command is written while the flag is set.
B0h	$\overline{\text{ORG}}$ sensor interrupt flag reset	The $\overline{\text{ORG}}$ sensor interrupt flag will be reset if this command is written while the flag is set.
B1h	$\overline{\text{EZ}}$ sensor interrupt flag reset	The $\overline{\text{EZ}}$ sensor interrupt flag will be reset if this command is written while the flag is set.
B2h	$\overline{\text{IN0}}$ input interrupt flag reset	The IN0 input interrupt flag will be reset if this command is written while the flag is set.
B3h	$\overline{\text{MARK}}$ input interrupt flag reset	The $\overline{\text{MARK}}$ input interrupt flag will be reset if this command is written while the flag is set.
B8h	Comparator (P = Q) interrupt flag reset	The comparator (P = Q) interrupt flag will be reset if this command is written while the flag is set.
B9h	Comparator (P > Q) interrupt flag reset	The comparator (P > Q) interrupt flag will be reset if this command is written while the flag is set.

Command code (hex)	Type	Description
E0h	$\overline{\text{OUT0}}$ set	Bit operation commands of the general-purpose output. Set the $\overline{\text{OUT0-7}}$ terminals to Low respectively.
E1h	$\overline{\text{OUT1}}$ set	
E2h	$\overline{\text{OUT2}}$ set	
E3h	$\overline{\text{OUT3}}$ set	
E4h	$\overline{\text{OUT4}}$ set	
E5h	$\overline{\text{OUT5}}$ set	
E6h	$\overline{\text{OUT6}}$ set	
E7h	$\overline{\text{OUT7}}$ set	
EEh	$\overline{\text{SON}}$ set	Sets servo ON output terminal $\overline{\text{SON}}$ to Low.

Command code (hex)	Type	Description
EFh	$\overline{\text{CLR}}$ output	When 1-shot is set, outputs the pulse for 32 reference clock periods from the CLR terminal. This terminal should be set to ON when the general-purpose output is set.
F0h	$\overline{\text{OUT0}}$ reset	Bit operation commands of the general-purpose output. Set the $\overline{\text{OUT0-7}}$ terminals to High respectively.
F1h	$\overline{\text{OUT1}}$ reset	
F2h	$\overline{\text{OUT2}}$ reset	
F3h	$\overline{\text{OUT3}}$ reset	
F4h	$\overline{\text{OUT4}}$ reset	
F5h	$\overline{\text{OUT5}}$ reset	
F6h	$\overline{\text{OUT6}}$ reset	
F7h	$\overline{\text{OUT7}}$ reset	
FEh	$\overline{\text{SON}}$ reset	Sets servo ON output terminal $\overline{\text{SON}}$ to High.
FFh	$\overline{\text{CLR}}$ reset	$\overline{\text{CLR}}$ should be reset to OFF when the general-purpose input is set.

4. Registers and Internal Counters

4-1 Register and Counter List

Table 4-1: Register and Counter List

Select code (hex)	Register and counter	Effective bit length	Setting range	Type	Higher address read /write
00h	Frequency multiplication ratio setting register (R_0)	12	1 to 4,096	Parameter	2-byte batch R/W
01h	Output pulse count setting register (counter C/R_1)	24	0 to 16,777,215	Parameter	3-byte batch R/W
02h	Deceleration start point setting register (counter D/R_2)	24	0 to 16,777,215 -8,388,608 to 8,388,607	Parameter	3-byte batch R/W
03h	Startup frequency setting register (R_3)	14	1 to 16,383 *1 1 to 10,000 *2	Parameter	2-byte batch R/W
04h	Maximum frequency setting register (R_4)	14	1 to 16,383 *1 1 to 10,000 *2	Parameter	2-byte batch R/W
05h	Accelerate rate setting register (R_5)	14	1 to 16,383	Parameter	2-byte batch R/W
06h	Deceleration rate setting register (R_6)	14	1 to 16,383	Parameter	2-byte batch R/W
07h	S-shaped acceleration/deceleration section setting register (R_7)	13	1 to 8,191	Parameter	2-byte batch R/W
08h	Linear interpolation base setting register (R_8)	24	1 to 16,777,215	Parameter	3-byte batch R/W
21h	Counter A	24/32		Counter	3/4-byte batch R/W
22h	Counter B	24/32		Counter	3/4-byte batch R/W
23h	Frequency read	14		Frequency	2-byte batch RD
30h	Comparator register	24	0 to 16,777,215 -8,388,608 to 8,388,607	Comparator	3-byte batch R/W
40h	Batch general-purpose output setting ($\overline{OUT0}$ to $\overline{7}$)	8		I/O	1-byte R/W
50h	Pulse output initial setting register	4		Initial setting	1-byte R/W
51h	Encoder input/output initial setting register	5		Initial setting	1-byte R/W
52h	Counter A initial setting register	7		Initial setting	1-byte R/W
53h	Counter B initial setting register	7		Initial setting	1-byte R/W
54h	Input initial setting register	6		Initial setting	1-byte R/W
55h	Input logic initial setting register	9		Initial setting	2-byte individual R/W
56h	Input filter initial setting register (F)	8		Initial setting	1-byte R/W
57h	Output initial setting register	1		Initial setting	1-byte R/W
58h	Output logic initial setting register	6		Initial setting	1-byte R/W
60h	Operation control mode setting register	6		Control mode	1-byte R/W
61h	Counter A control mode setting register	2		Control mode	1-byte R/W
62h	Counter B control mode setting register	2		Control mode	1-byte R/W
63h	CLR output control mode setting register	2		Control mode	1-byte R/W
64h	Comparator control mode setting register	6		Control mode	1-byte R/W
70h	Pulse oscillation interrupt mask register	5		Interrupt	1-byte R/W
71h	Counter interrupt mask register	5		Interrupt	1-byte R/W
72h	Sensor interrupt mask register	4		Interrupt	1-byte R/W
73h	Comparator interrupt mask register	2		Interrupt	1-byte R/W
E0h	Pulse oscillation interrupt flag register	5		Interrupt	1-byte RD
E1h	Counter interrupt flag register	5		Interrupt	1-byte RD
E2h	Sensor interrupt flag register	4		Interrupt	1-byte RD
E3h	Comparator interrupt flag register	2		Interrupt	1-byte RD

Select code (hex)	Register and counter	Effective bit length	Setting range	Type	Higher address read /write
F0h	Sensor status register	8		Status	2-byte individual RD
F1h	Normal stop factor status register	6		Status	1-byte RD
F2h	Error stop factor status register	3		Status	1-byte RD
F3h	General-purpose input status register	8		Status	1-byte RD
F4h	Comparator status register	2		Status	1-byte RD

*1:Linear acceleration/deceleration mode or deceleration start point manual setting mode.

*2:S-shaped acceleration/deceleration mode or deceleration start point automatic calculation mode.

R/W: Read and Write RD: Read only

4-2 Read/Write of Registers and Counters

The reading/writing of the registers and counters in Table 4-1 writes the select code to the register selector in Table 2-1 Address Allocation Table, and reads or writes data 1 to 4.

4-2-1 Read/Write of a 1-byte Register

To read a register, write the select code in the register selector and read data from read data 1.

To write a register, write the select code in the register selector and write data in write data 1.

4-2-2 Read/Write of a 2-byte Register

To read a register, write the select code in the register selector, read the lower byte (bits 0 to 7) from read data 1, and then read the higher byte (bits 8 to 15) from read data 2.

To write a register, write the select code in the register selector, write the lower byte (bits 0 to 7) write data 1, and then write the higher byte (bits 8 to 15) in write data 2.

4-2-3 Read/Write of a 3-byte Register or Counter

To read a register or counter, write the select code in the register selector, read the lowest byte (bits 0 to 7) from read data 1, then read the intermediate byte (bits 8 to 15) from read data 2, and read the highest byte (bits 16 to 23) from read data 3.

To write a register or counter, write the select code in the register selector, write the lowest byte (bits 0 to 7) in write data 1, then write the intermediate byte (bits 8 to 15) in write data 2, and write the highest byte (bits 16 to 23) in write data 3.

4-2-4 Read/write of a 4-byte Counter

To read a 4-byte counter, write the select code in the register selector, read the lowest byte (bits 0 to 7) from read data 1, then read the intermediate byte (bits 8 to 15) from read data 2, read the next intermediate byte (bits 16 to 23) from read data 3, and read the highest byte (bits 24 to 31) from read data 4.

To write data in a 4-byte counter, write the select code in the register selector, write the lowest byte (bits 0 to 7) in write data 1, then write the intermediate byte (bits 8 to 15) in write data 2, write the next intermediate byte (bits 16 to 23) in write data 3, and write the highest byte (bits 24 to 31) in write data 4.

5. Parameters Related to Pulse Output

The LSI has 9 parameters for use in pulse output and timer operations. These parameters can be set with parameter registers R_0 to R_8.

5-1 Parameter Types

5-1-1 Frequency Multiplication Ratio Setting Register (Register R_0)

Register R_0 is used to set the multiplication range of the output frequency. The setting range is between 1 and 4096, but it should be set at 0 for 4096. Table 5-1 shows the setting, multiplication ratio [pps/step] and output frequency range of register R_0.

Table 5-1: Frequency Multiplication Ratio and Output Frequency Range (Reference clock f = 1 6.384 MHz)

R_0	Multiplication ratio [pps/step]	Output frequency range [pps]	
		Linear acceleration/ deceleration	S-shaped acceleration/ deceleration
2500	0.1	0.1 to 1,638.3	0.1 to 1,000
250	1	1 to 16,383	1 to 10,000
50	5	5 to 81,915	5 to 50,000
10	25	25 to 409,575	25 to 250,000
1	250	250 to 4,095,750	250 to 2,500,000

5-1-2 Output Pulse Count Setting Register (Register R_1)

Register R_1 is used to set the number of output pulses. As register R_1 is also common as counter C, writing register R_1 results in presetting counter C. The value of counter C when the pulse output is forced to stop in the middle is (register R_1 set value - output pulse count). When outputting only the remaining number of pulses the next time, there is no need to reset. In other cases, the R_1 register must be set each time.

5-1-3 Deceleration Start Point Setting Register (Register R_2)

Although the LSI is provided with the automatic deceleration start point calculation mode, the deceleration start point can be set manually or the offset for it can be set by writing data in register R_2.

Register R_2 is also common as counter D, but the count operation is not performed when the register is used in the deceleration start point manual setting mode.

5-1-4 Startup Frequency Setting Register (Register R_3)

This is the parameter register for determining the frequency at the start and end of pulse output.

5-1-5 Maximum Frequency Setting Register (Register R_4)

This is the parameter register determining the maximum frequency of the pulse output. In the linear acceleration/ deceleration and deceleration start point automatic calculation modes, it can be rewritten even during pulse output. In the case of S-shaped acceleration/deceleration, overwriting in the middle is possible during constant speed in continuous mode and deceleration start point manual setting mode.

5-1-6 Acceleration Rate Setting Register (Register R_5)

This is the parameter register for determining the acceleration rate.

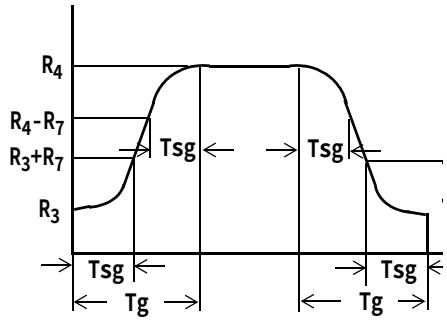
5-1-7 Deceleration Rate Setting Register (Register R_6)

This is the parameter register for determining the deceleration rate. Registers R_5 and R_6 should be set to the same value for the deceleration start point automatic calculation mode.

5-1-8 S-shaped Acceleration/Deceleration Section Setting Register (Register R_7)

The S-shaped acceleration/deceleration sections refer to sections Tsg shown in Figure 5-1. In the sections between R_3 and (R_3+R_7) and between (R_4-R_7) and R_4, the speed varies by drawing S-shaped curves. The set value of register R_7 should be no more than $(R_4-R_3)/2$. The register need not be set when the S-shaped acceleration/ deceleration are not used.

Figure 5-1:S-shaped Acceleration/Deceleration Condition



5-1-9 Linear Interpolation Base Setting Register (Register R_8)

When using multiple axes or more than one LSI to carry out linear interpolation drive, set the register R_1 setting value of the axes with the greatest amount of movement in register R_8. There is no need to set it if linear interpolation drive will not be used.

5-2 Parameter Calculation Formulae

Table 5-2: Parameter Calculation Formulae

Speed resolution [factor] K [pps/step]	$K = \frac{f}{65,536 \times R_0}$ f: Reference clock frequency [Hz]
Startup frequency V [pps]	Stand alone mode: $V = \frac{f \times R_3}{65,536 \times R_0}$ Linear interpolation mode: $V = \frac{f \times R_3 \times R_1}{65,536 \times R_0 \times R_8}$
Maximum frequency V [pps]	Stand alone mode: $V = \frac{f \times R_4}{65,536 \times R_0}$ Linear interpolation mode: $V = \frac{f \times R_4 \times R_1}{65,536 \times R_0 \times R_8}$
Acceleration rate g [pps/sec]	Stand alone mode: $g = \frac{f \times K \times R_5}{131,072}$ Linear interpolation mode: $g = \frac{f \times K \times R_5 \times R_1}{131,072 \times R_8}$
Deceleration rate g [pps/sec]	Stand alone mode: $g = \frac{f \times K \times R_6}{131,072}$ Linear interpolation mode: $g = \frac{f \times K \times R_6 \times R_1}{131,072 \times R_8}$
Acceleration/ deceleration time (linear) Tg [sec]	(Acceleration) $Tg = \frac{131,072 \times (R_4 - R_3)}{f \times R_5}$ (Deceleration) $Tg = \frac{131,072 \times (R_4 - R_3)}{f \times R_6}$
Acceleration/ deceleration time (sine) Tg [sec]	(Acceleration) $Tg = \frac{131,072 \times (R_4 - R_3 - 2 \times R_7 + \pi \times R_7)}{f \times R_5}$ (Deceleration) $Tg = \frac{131,072 \times (R_4 - R_3 - 2 \times R_7 + \pi \times R_7)}{f \times R_6}$
Acceleration/ deceleration time (parabolic) Tg [sec]	(Acceleration) $Tg = \frac{131,072 \times (R_4 - R_3 + 2 \times R_7)}{f \times R_5}$ (Deceleration) $Tg = \frac{131,072 \times (R_4 - R_3 + 2 \times R_7)}{f \times R_6}$
Deceleration start point (linear) Dp [pulses]	For rapezo(when R4 > R3): $Dp = \frac{(R_4 - R_3)(R_4 + R_3 - 1)}{R_0 \times R_6}$ Triangular drive: $Dp = \frac{R_1 \times R_5}{R_5 + R_6}$
Deceleration start point (sine) Dp [pulses]	For rapezo (when R4 > R3): $Dp = \frac{(R_4 - R_3 - 2 \times R_7 + \pi \times R_7)(R_4 + R_3)}{R_0 \times R_6}$ Triangular drive: $Dp = \frac{R_1 \times R_5}{R_5 + R_6}$

Table 5-2: Parameter Calculation Formulae

Deceleration start point (parabolic) Dp [pulses]	**For rapezo (when R4 > R3):** $Dp = \frac{(R_4 - R_3 + 2 \times R_7 - 2)(R_4 + R_3)}{R_0 \times R_6}$ **Triangular drive:** $Dp = \frac{R_1 \times R_5}{R_5 + R_6}$

π =Ratio of the circumference of a circle to its diameter

6. Initial Setting Registers

The initial setting registers must be set after the power ON reset. After that, the setting can be changed while pulse output is stopping.

6-1 Functions of Initial Setting Registers

6-1-1 Pulse Output Initial Setting Register

Table 6-1: Pulse Output Initial Setting Register

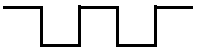
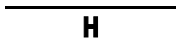
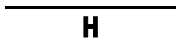
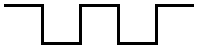
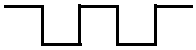
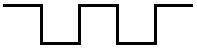
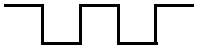
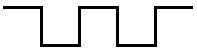
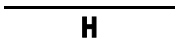
bit	Description	
	0	1
0	0.5 pulse idling	1.5 pulse idling
1	Undefined (0 should be set)	
2	+ direction is CW pulse output	+ direction is CCW pulse output
3	CW/CCW 2-clock system	PULSE/DIR gate system
4	Undefined (0 should be set)	
5	Undefined (0 should be set)	
6	Undefined (0 should be set)	
7	Operation completion flag is set to ON when the pulse output has completed	Operation completion flag is set to ON when positioning has completed.

Idling

The idling function allows delay acceleration or deceleration. When it is set to 0, acceleration starts in 0.5 pulse after the startup and deceleration ends 0.5 pulse before the stopping of the pulse. When it is set to 1, acceleration starts in 1.5 pulses after the startup and deceleration ends 1.5 pulses before the stopping of the pulse.

$\overline{\text{POUT}}$ and $\overline{\text{PDIR}}$ outputs

Table 6-2: Pulse Output Initial Setting and $\overline{\text{POUT/PDIR}}$ Outputs

bit3	bit2	$\overline{\text{POUT}}$		$\overline{\text{PDIR}}$	
		+	−	+	−
0	0				
0	1				
1	0				
1	1				

Note: Inverts in the case of positive logic.

Operation completion flag

The operation completion flag can be read in the operation status byte. When bit 7 = 0, the operation completion flag becomes 1 immediately after the completion of the pulse output. When bit 7 = 1, the flag becomes 1 when the $\overline{\text{INP}}$ input terminal becomes active after the completion of the pulse output.

6-1-2 Encoder Input/Output Initial Setting Register

Table 6-3: Encoder Input/Output Initial Setting Register

bit	Description	
	0	1
0	$\overline{EA}$, $\overline{EB}$ input mode code 1	
1	$\overline{EA}$, $\overline{EB}$ input mode code 2	
2	Undefined (0 should be set)	
3	Undefined (0 should be set)	
4	Undefined (0 should be set)	
5	Undefined (0 should be set)	
6	Undefined (0 should be set)	
7	Undefined (0 should be set)	

Encoder input mode codes

Table 6-4: Encoder Input Mode Codes

Code 2	Code 1	Description
0	0	2 clocks, negative logic
0	1	2-phase clock, x 4 multiplication
1	0	2-phase clock, x 2 multiplication
1	1	2-phase clock, x 1 multiplication

6-1-3 Counter A/B Initial Setting Register

Table 6-5: Counter A/B Initial Setting Register

bit	Description	
	0	1
0	Internal oscillation pulse count disable	Internal oscillation pulse count enable
1	Encoder count disable	Encoder count enable
2	Undefined (0 should be set)	
3	Encoder input forward count	Encoder input reverse count
4	Undefined (0 should be set)	
5	Count between -8,388,608 and 8,388,607	Count between 0 and 16,777,215
6	24-bit mode	32-bit mode
7	Undefined (0 should be set)	

Multiplex input count

Counters A and B can simultaneously count internal oscillation pulses and encoder input. The counts can be enabled with bits 0 to 1.

The forward count of the encoder input of bit 3 refers to counting upward when phase A precedes phase B and counting downward when phase B precedes phase A. The opposite results when the reverse count setting is made.

6-1-4 Input Initial Setting Register

Table 6-6: Input Initial Setting Register

bit	Description	
	0	1
0	$\overline{+SLD}$ and $\overline{-SLD}$ are deceleration inputs	$\overline{+SLD}$ and $\overline{-SLD}$ are deceleration stop inputs
1	$\overline{+SLD}$ and $\overline{-SLD}$ are level operation inputs	$\overline{+SLD}$ and $\overline{-SLD}$ are edge operation inputs
2	$\overline{ORG}$ is a low-sensitivity input	$\overline{ORG}$ is a high-sensitivity input
3	$\overline{MARK}$ is a low-sensitivity input	$\overline{MARK}$ is a high-sensitivity input
4	$\overline{CLRA}$ is the level clear input	$\overline{CLRA}$ is the edge clear input
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

When bit 0 = 0 and $\overline{+SLD}$ or $\overline{-SLD}$ goes active, the drive decelerates to the speed set with register R_3 (in the case that $R_4 > R_3$) and the pulse continues to be output. When bit 0 = 1 and $\overline{+SLD}$ or $\overline{-SLD}$ goes active, the drive decelerates to the speed set with register R_3 and the pulse output is stopped.

6-1-5 Input Logic Initial Setting Registers I and II

Input logic initial setting register I performs read/write of data 1 shown in Table 2-1, while input logic initial setting register II performs read/write of data 2 in the same table.

Table 6-7: Input Logic Initial Setting Register I

bit	Description	
	0	1
0	$\overline{+EL}$ is a negative logic input	$\overline{+EL}$ is a positive logic input
1	$\overline{-EL}$ is a negative logic input	$\overline{-EL}$ is a positive logic input
2	$\overline{ALM}$ is a negative logic input	$\overline{ALM}$ is a positive logic input
3	Not used (permanently set to 0)	
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

Table 6-8: Input Logic Initial Setting Register II

bit	Description	
	0	1
0	$\overline{\text{ORG}}$ is negative logic	$\overline{\text{ORG}}$ is positive logic
1	$\overline{\text{EZ}}$ is negative logic	$\overline{\text{EZ}}$ is positive logic
2	$\overline{\text{+SLD}}$ is a negative logic input	$\overline{\text{+SLD}}$ is a positive logic input
3	$\overline{\text{-SLD}}$ is a negative logic input	$\overline{\text{-SLD}}$ is a positive logic input
4	$\overline{\text{INP}}$ is a negative logic input	$\overline{\text{INP}}$ is a positive logic input
5	$\overline{\text{MARK}}$ is a negative logic input	$\overline{\text{MARK}}$ is a positive logic input
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

6-1-6 Initial Setting Register (F) for Input Filter

The setting values of the input filter decides the sensitivity of $\overline{\text{+EL}}$, $\overline{\text{-EL}}$, $\overline{\text{ALM}}$, $\overline{\text{+SLD}}$ and $\overline{\text{-SLD}}$. The setting value range is from 1 to 256. Set 0 for 256.

Sensitivity is one cycle of 16 x F x reference clock.

6-1-7 Initial Setting Register for Output

Table 6-9: Initial Setting Register for Output

bit	Description	
	0	1
0	$\overline{\text{CLR}}$ is 1-shot output	$\overline{\text{CLR}}$ is general-purpose output
1	Undefined (permanently set to 0)	
2	Undefined (permanently set to 0)	
3	Undefined (permanently set to 0)	
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

6-1-8 Initial Setting Register for Output Logic

Table 6-10: Initial Setting Register for Output Logic

bit	Description	
	0	1
0	$\overline{\text{POUT}}$ is a negative logic output	$\overline{\text{POUT}}$ is a positive logic output
1	$\overline{\text{PDIR}}$ is a negative logic output	$\overline{\text{PDIR}}$ is a positive logic output
2	$\overline{\text{CLR}}$ is a negative logic output	$\overline{\text{CLR}}$ is a positive logic output
3	$\overline{\text{INT}}$ is a negative logic output	$\overline{\text{INT}}$ is a positive logic output
4	$\overline{\text{ERROR}}$ is a negative logic output	$\overline{\text{ERROR}}$ is a positive logic output
5	$\overline{\text{MOVE}}$ is a negative logic output	$\overline{\text{MOVE}}$ is a positive logic output
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

There is no setting of ERROR and MOVE for bit 4 and 5 for X7083.

7. Control Mode Registers

7-1 Functions of Control Mode Registers

7-1-1 Operation Control Mode Setting Register

Table 7-1: Operation Control Mode Setting Register

bit	Description	
	0	1
0	Sync start control is disabled	Sync start control is enabled
1	Deceleration start point control code 1	
2	Deceleration start point control code 2	
3	Interpolation control is disabled	Interpolation control is enabled
4	Linear acceleration/deceleration mode	S-shaped acceleration/deceleration mode
5	Parabolic	Sine
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

Sync start

When the sync start control is enabled, the pulse oscillation or timer count starts when sync start input terminal $\overline{\text{SYNC}}$ changes from High to Low after one of the drive commands 00h to 19h or a timer command 40h or 41h has been written.

Deceleration start point control codes

The deceleration start point control has 4 modes as shown below. These modes are set with bits 1 and 2.

Code 2	Code 1	Description
0	0	Automatic calculation mode
0	1	Offset setting mode
1	0	Manual setting mode
1	1	No deceleration mode

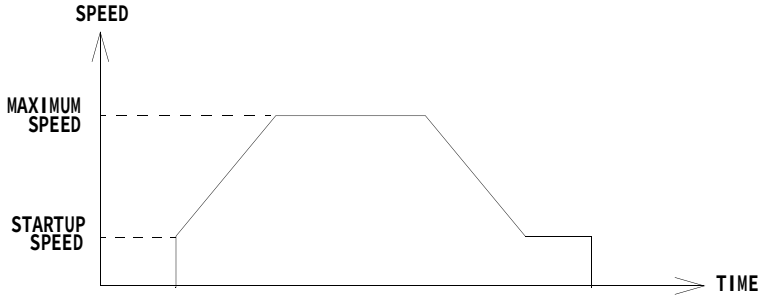
Automatic calculation

This mode can be used when the acceleration rate and deceleration rate are identical. Counter D is cleared to 0 at the start of drive and counting is performed during drive. When the value of remaining pulse count management counter C becomes equal to or less than the value of counter D, the drive starts to decelerate. Counter D need not be preset before the startup.

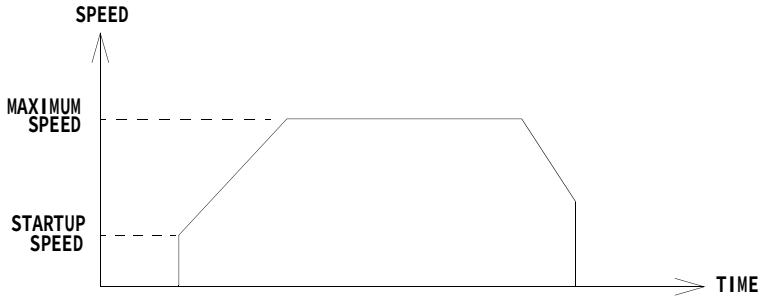
Offset setting

In this mode, counter D is not cleared to 0 at the start of drive and counting is performed during drive. When the value of remaining pulse count management counter C becomes equal to, or less than, the value of counter D, the drive starts to decelerate. The offset value should be preset before starting the drive. The setting value is between -8,388,608 and 8,388,607 and preset in counter D in the form of 2 complement. The operations that occur are shown below.

When a positive value is preset:



When a negative value is preset:

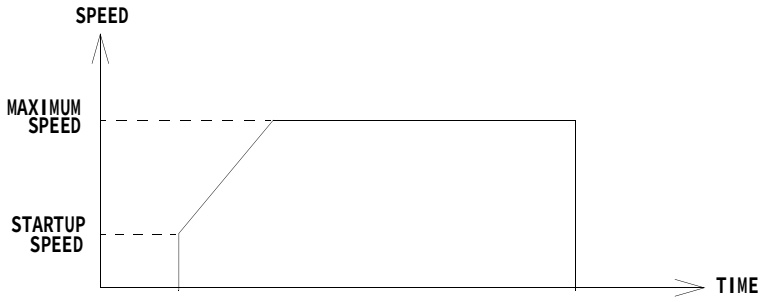


Manual setting

In this mode, deceleration start point management counter D does not perform counting but functions as register R_2. It is not cleared to 0 at the start of drive. The drive starts to decelerate when the value of remaining pulse count management counter C becomes equal to, or less than, the preset value of register R_2.

No deceleration start point operation performed

The operation in this mode is as shown below.



S-shaped acceleration/deceleration

In the S-shaped acceleration/deceleration mode that is set with bit 4 = 1, two kinds of acceleration/deceleration shapes can be used. Namely, the parabolic curve can be used when bit 5 = 0 and the sine functional curve can be used when bit 5 = 1.

7-1-2 Counter A and B Control Register

Table 7-2: Counter A and B Control Register

bit	Description	
	0	1
0	Automatic clear does not occur after error stop	Automatic clear occurs after error stop
1	Automatic clear does not occur after normal stop	Automatic clear occurs after normal stop
2	Undefined (permanently set to 0)	
3	Undefined (permanently set to 0)	
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

7-1-3 $\overline{\text{CLR}}$ Output Control Mode Register

Table 7-3: $\overline{\text{CLR}}$ Output Control Mode Register

bit	Description	
	0	1
0	CLR is not output automatically after error stop	CLR is output automatically after error stop
1	CLR is not output automatically after normal stop	CLR is output automatically after normal stop
2	Undefined (permanently set to 0)	
3	Undefined (permanently set to 0)	
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

7-1-4 Comparator Control Mode Register

Table 7-4: Comparator Control Mode Register

bit	Description	
	0	1
0	P input select code 1	
1	P input select code 2	
2	Undefined (0 should be set)	
3	Q input select code 1	
4	Q input select code 2	
5	Undefined (0 should be set)	
6	Absolute value comparison	2 complement comparison
7	Comparator output is P = Q	Comparator output is P > Q

There is no setting of comparator output on bit7 for X7083.

Input select code (common to P and Q)

Code 2	Code 1	Description
0	0	Counter A
0	1	Counter B
1	0	Counter C
1	1	Comparator register

8. Interrupt Function

The LSI has an interrupt function based on the pulse output, counter and sensor factors. It is also possible to mask the interrupt due to each factor.

8-1 Interrupt Mask Registers

8-1-1 Pulse Oscillation Interrupt Mask Register

Table 8-1: Pulse Oscillation Interrupt Mask Register

bit	Description	
	0	1
0	Normal pulse output completion interrupt disabled	Normal pulse output completion interrupt enabled
1	Error stop interrupt disabled	Error stop interrupt enabled
2	Deceleration start point interrupt disabled	Deceleration start point interrupt enabled
3	ISO-speed interrupt disabled	ISO-speed interrupt enabled
4	Not used (permanently set to 0)	
5	Maximum acceleration rate interrupt disabled	Maximum acceleration rate interrupt enabled
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

8-1-2 Counter Interrupt Mask Register

Table 8-2: Counter Interrupt Mask Register

bit	Description	
	0	1
0	Counter A carry interrupt disabled	Counter A carry interrupt enabled
1	Counter A borrow interrupt disabled	Counter A borrow interrupt enabled
2	Counter B carry interrupt disabled	Counter B carry interrupt enabled
3	Counter B borrow interrupt disabled	Counter B borrow interrupt enabled
4	Undefined (permanently set to 0)	
5	Counter C borrow interrupt disabled	Counter C borrow interrupt enabled
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

8-1-3 Sensor Interrupt Mask Register

Table 8-3: Sensor Interrupt Mask Register

bit	Description	
	0	1
0	$\overline{\text{ORG}}$ interrupt disabled	$\overline{\text{ORG}}$ interrupt enabled
1	$\overline{\text{EZ}}$ interrupt disabled	$\overline{\text{EZ}}$ interrupt enabled
2	$\overline{\text{IN0}}$ interrupt disabled	$\overline{\text{IN0}}$ interrupt enabled
3	$\overline{\text{MARK}}$ interrupt disabled	$\overline{\text{MARK}}$ interrupt enabled
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

8-1-4 Comparator Interrupt Mask Register

Table 8-4: Comparator Interrupt Mask Register

bit	Description	
	0	1
0	P = Q interrupt disabled	P = Q interrupt enabled
1	P > Q interrupt disabled	P > Q interrupt enabled
2	Undefined (permanently set to 0)	
3	Undefined (permanently set to 0)	
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

8-2 Interrupt Flag Registers

8-2-1 Pulse Oscillation Interrupt Flag Register

Table 8-5: Pulse Oscillation Interrupt Flag Register

bit	Description	
	0	1
0	Pulse output completion interrupt flag is OFF	Pulse output completion interrupt flag is ON
1	Error stop interrupt flag is OFF	Error stop interrupt flag is ON
2	Deceleration start point interrupt flag is OFF	Deceleration start point interrupt flag is ON
3	ISO-speed interrupt flag is OFF	ISO-speed interrupt flag is ON
4	Undefined (permanently set to 0)	
5	Maximum acceleration rate interrupt flag is OFF	Maximum acceleration rate interrupt flag is ON
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

8-2-2 Counter Interrupt Flag Register

Table 8-6: Counter Interrupt Flag Register

bit	Description	
	0	1
0	Counter A carry interrupt flag is OFF	Counter A carry interrupt flag is ON
1	Counter A borrow interrupt flag is OFF	Counter A borrow interrupt flag is ON
2	Counter B carry interrupt flag is OFF	Counter B carry interrupt flag is ON
3	Counter B borrow interrupt flag is OFF	Counter B borrow interrupt flag is ON
4	Undefined (permanently set to 0)	
5	Counter C borrow interrupt flag is OFF	Counter C borrow interrupt flag is ON
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

8-2-3 Sensor Interrupt Flag Register

Table 8-7: Sensor Interrupt Flag Register

bit	Description	
	0	1
0	$\overline{\text{ORG}}$ interrupt flag is OFF	$\overline{\text{ORG}}$ interrupt flag is ON
1	$\overline{\text{EZ}}$ interrupt flag is OFF	$\overline{\text{EZ}}$ interrupt flag is ON
2	$\overline{\text{IN0}}$ interrupt flag is OFF	$\overline{\text{IN0}}$ interrupt flag is ON
3	$\overline{\text{MARK}}$ interrupt flag is OFF	$\overline{\text{MARK}}$ interrupt flag is ON
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

8-2-4 Comparator Interrupt Flag Register

Table 8-8: Comparator Interrupt Flag Register

bit	Description	
	0	1
0	P = Q interrupt flag is OFF	P = Q interrupt flag is ON
1	P > Q interrupt flag is OFF	P > Q interrupt flag is ON
2	Undefined (permanently set to 0)	
3	Undefined (permanently set to 0)	
4	Undefined (permanently set to 0)	
5	Undefined (permanently set to 0)	
6	Undefined (permanently set to 0)	
7	Undefined (permanently set to 0)	

9. Status Registers

Status registers consist of a main status — i.e. operation status and interrupt status that can be read in Table 2-1 Address Allocation Table — and an auxiliary status that sets the register selector and then reads using read data 1 to 3.

9-1 Main Status

9-1-1 Operation Status

The operation status register shows the most comprehensive status of the LSI. The status contents include the pulse output condition, the pulse output end condition, and whether interrupt is used or not.

Table 9-1: Operation Status

bit	Description	
	0	1
0	Stopping	Operating
1	Not accelerating	Accelerating
2	Not decelerating	Decelerating
3	Undefined (permanently set to 0)	
4	Error flag is OFF	Error flag is ON
5	Stop flag is OFF	Stop flag is ON
6	Interrupt flag is OFF	Interrupt flag is ON
7	$\overline{\text{CLR}}$ is OFF	$\overline{\text{CLR}}$ is ON

9-1-2 Interrupt Status

The interrupt status register allows you to identify the group to which the current interrupt belongs. Detailed interrupt factors can be identified by reading the interrupt flag register.

Table 9-2: Interrupt Status

bit	Description	
	0	1
0	Pulse oscillation interrupt flag is OFF	Pulse oscillation interrupt flag is ON
1	Counter interrupt flag is OFF	Counter interrupt flag is ON
2	Sensor interrupt flag is OFF	Sensor interrupt flag is ON
3	Comparator interrupt flag is OFF	Comparator interrupt flag is ON
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

9-1-3 Interrupt Axis Status

The interrupt axis status allows you to identify which axis is generating an interrupt.

Table 9-3: Interrupt Axis Status

bit	Description	
	0	1
0	Axis #1interrupt flag is OFF	Axis #1interrupt flag is ON
1	Axis #2 interrupt flag is OFF	Axis #2 interrupt flag is ON
2	Axis #3 interrupt flag is OFF	Axis #3 interrupt flag is ON
3	Axis #4 interrupt flag is OFF	Axis #4 interrupt flag is ON
4	Axis #5 interrupt flag is OFF	Axis #5 interrupt flag is ON
5	Axis #6 interrupt flag is OFF	Axis #6 interrupt flag is ON
6	Axis #7 interrupt flag is OFF	Axis #7 interrupt flag is ON
7	Axis #8 interrupt flag is OFF	Axis #8 interrupt flag is ON

.Axes #1 to #4 for X7043; axes #1 to #2 are for X7023.

9-2 Auxiliary Status

9-2-1 Sensor Status

The sensor status registers allow you to read the conditions of the sensor input in real time. It is a 2-byte, individually read register. When the register selector shown in Table 2-1 Address Allocation Table is written, read data 1 allows the reading of the status of +EL, -EL and ALM, and read data 2 allows the reading of the status of ORG, EZ, +SLD, -SLD, INP and MARK.

Table 9-4: Sensor Status 1

bit	Description	
	0	1
0	+EL is OFF	+EL is ON
1	-EL is OFF	-EL is ON
2	ALM is OFF	ALM is ON
3	Not used (permanently set to 0)	
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

Table 9-5: Sensor Status 2

bit	Description	
	0	1
0	ORG is OFF	ORG is ON
1	EZ is OFF	EZ is ON
2	+SLD is OFF	+SLD is ON
3	-SLD is OFF	-SLD is ON
4	INP is OFF	INP is ON
5	MARK is OFF	MARK is ON
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

9-2-2 Normal Stop Factor Status

The normal stop factor status register allows you to identify the stop factor when the stop flag of the operation status is ON and the error flag of the operation status is OFF. The stop is due to the completion of the return-to-origin operation if ORG and EZ are ON, and due to the deceleration stop by the sensor if +SLD or -SLD is ON.

Table 9-6: Normal Stop Factor Status

bit	Description	
	0	1
0	ORG is OFF	ORG is ON
1	EZ is OFF	EZ is ON
2	+SLD is OFF	+SLD is ON
3	-SLD is OFF	-SLD is ON
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

9-2-3 Error Stop Factor Status

The error stop factor status register allows you to identify the stop factor when both the stop and error flags of the operation status are ON.

Table 9-7: Error Stop Factor Status

bit	Description	
	0	1
0	+EL is OFF	+EL is ON
1	-EL is OFF	-EL is ON
2	ALM is OFF	ALM is ON
3	Not used (permanently set to 0)	
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

9-2-4 General-Purpose Input Status

The general-purpose input status register allows you to identify the conditions of the $\overline{\text{IN0 to 7}}$ inputs in real time.

Table 9-8: General-Purpose Input Status

bit	Description	
	0	1
0	$\overline{\text{IN0}}$ is OFF	$\overline{\text{IN0}}$ is ON
1	$\overline{\text{IN1}}$ is OFF	$\overline{\text{IN1}}$ is ON
2	$\overline{\text{IN2}}$ is OFF	$\overline{\text{IN2}}$ is ON
3	$\overline{\text{IN3}}$ is OFF	$\overline{\text{IN3}}$ isON
4	$\overline{\text{IN4}}$ is OFF	$\overline{\text{IN4}}$ is ON
5	$\overline{\text{IN5}}$ is OFF	$\overline{\text{IN5}}$ is ON
6	$\overline{\text{IN6}}$ is OFF	$\overline{\text{IN6}}$ is ON
7	$\overline{\text{IN7}}$ is OFF	$\overline{\text{IN7}}$ is ON

9-2-5 Comparator Status

The comparator status shows the result of comparison between the P and Q inputs set with the comparator control mode setting register.

Table 9-9: Comparator Status

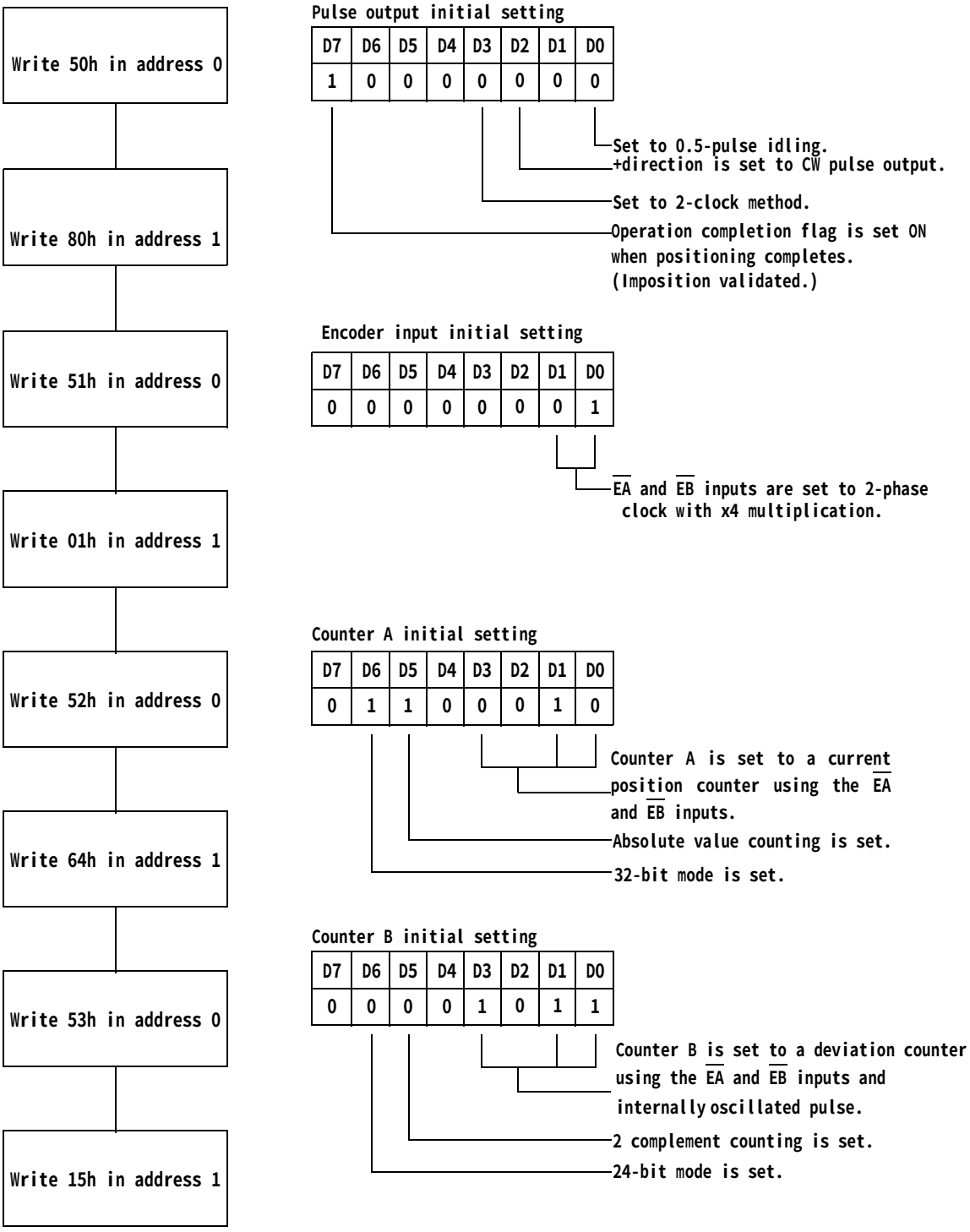
bit	Description	
	0	1
0	P is not equal to Q	P = Q
1	P is not larger than Q	P > Q
2	Not used (permanently set to 0)	
3	Not used (permanently set to 0)	
4	Not used (permanently set to 0)	
5	Not used (permanently set to 0)	
6	Not used (permanently set to 0)	
7	Not used (permanently set to 0)	

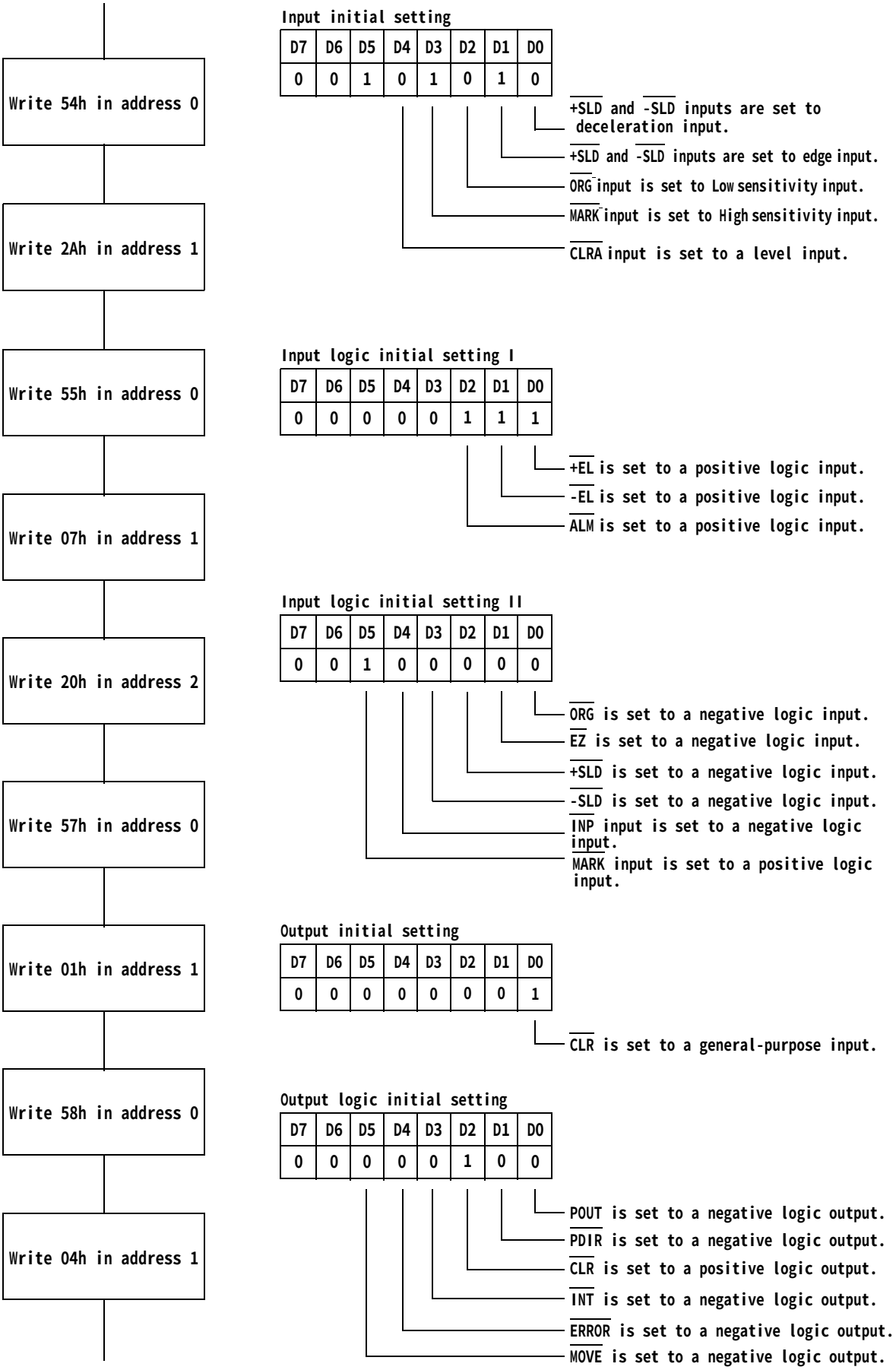
10. Application Example

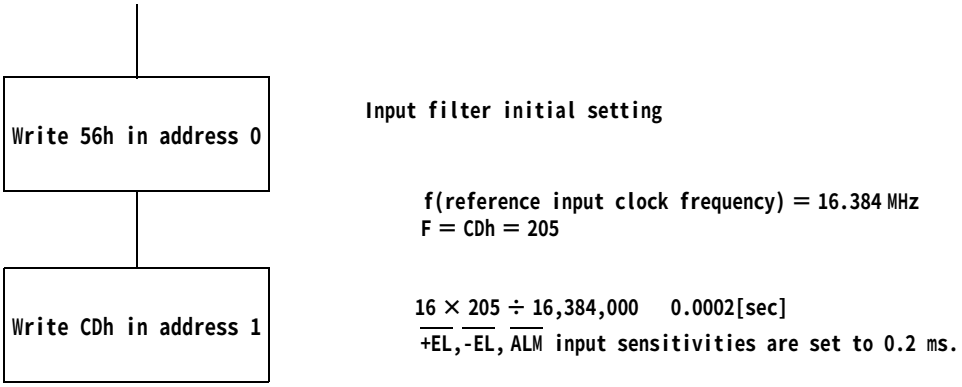
10-1 Initial Setting

After power ON resetting, the eight initial setting registers must be set once. They do not need to be set in any particular order.

Figure 10-1: Initial Setting Flow Chart (for Axis #1)



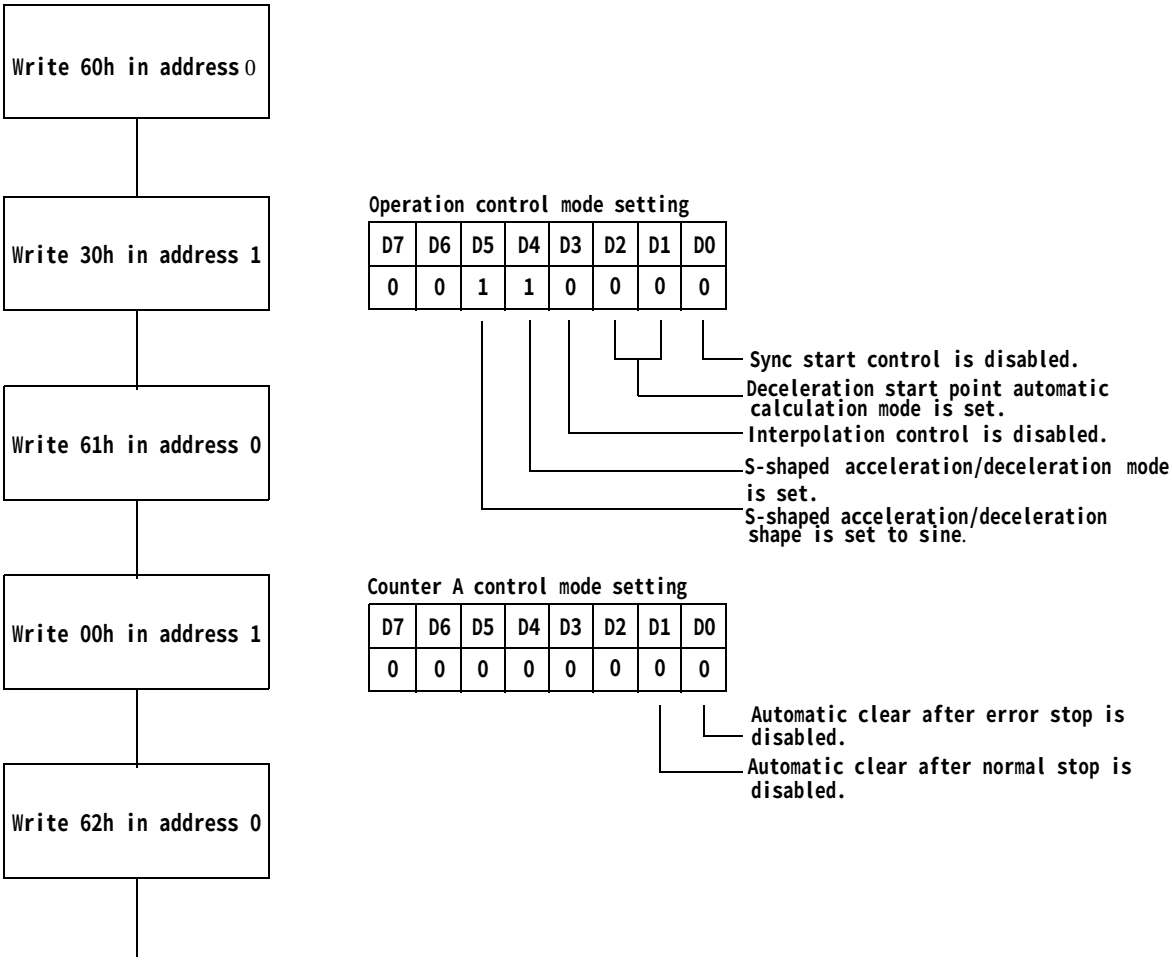

Write 54h in address 0
Write 2Ah in address 1
Write 55h in address 0
Write 07h in address 1
Write 20h in address 2
Write 57h in address 0
Write 01h in address 1
Write 58h in address 0
Write 04h in address 1
Input initial setting
D7 D6 D5 D4 D3 D2 D1 D0
0 0 1 0 1 0 1 0
+SLD and -SLD inputs are set to deceleration input.
+SLD and -SLD inputs are set to edge input.
ORG input is set to Low sensitivity input.
MARK input is set to High sensitivity input.
CLRA input is set to a level input.
Input logic initial setting I
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 1 1 1
+EL is set to a positive logic input.
-EL is set to a positive logic input.
ALM is set to a positive logic input.
Input logic initial setting II
D7 D6 D5 D4 D3 D2 D1 D0
0 0 1 0 0 0 0 0
ORG is set to a negative logic input.
EZ is set to a negative logic input.
+SLD is set to a negative logic input.
-SLD is set to a negative logic input.
INP input is set to a negative logic input.
MARK input is set to a positive logic input.
Output initial setting
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 0 0 1
CLR is set to a general-purpose input.
Output logic initial setting
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 1 0 0
POUT is set to a negative logic output.
PDIR is set to a negative logic output.
CLR is set to a positive logic output.
INT is set to a negative logic output.
ERROR is set to a negative logic output.
MOVE is set to a negative logic output.

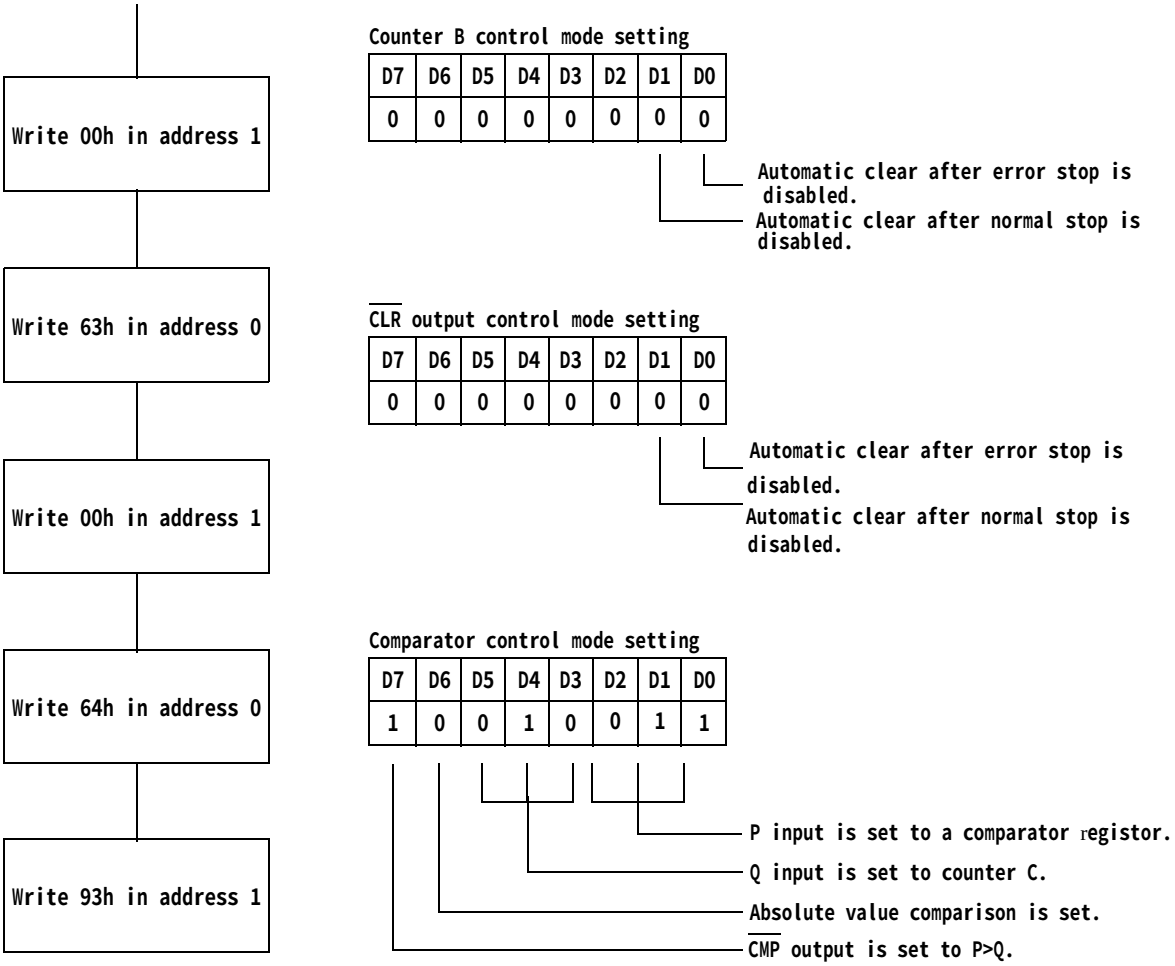


10-2 Control Mode Setting

After the power ON resetting, the control mode must be set at least once before starting the drive. There is no particular setting order, but you should change the operation mode setting register before setting the R_1 register and the R_8 register. Resetting is not required unless the control mode is to be changed.

Figure 10-2: Control Mode Setting Flow Chart (for Axis #1)

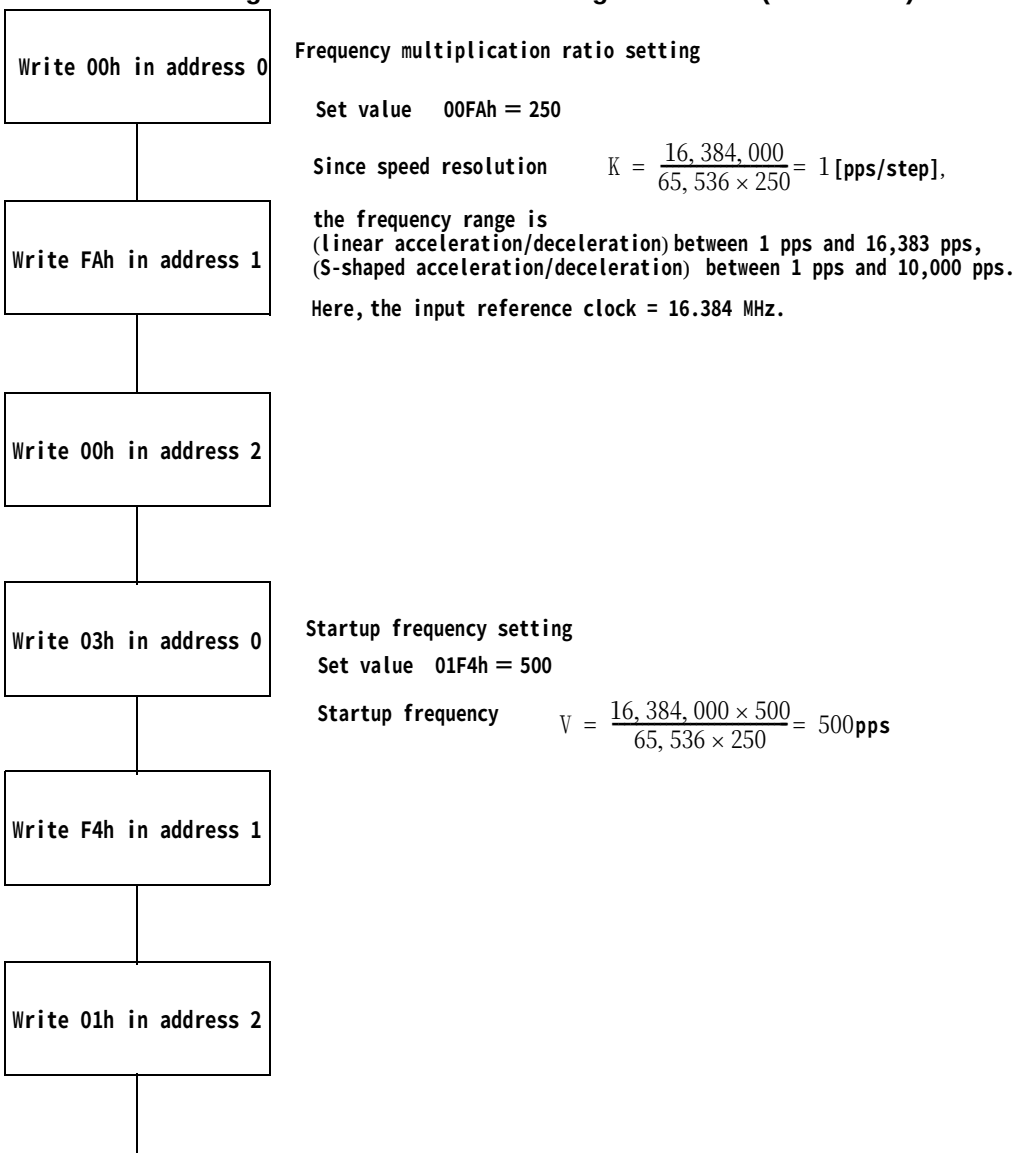



Write 00h in address 1
Write 63h in address 0
Write 00h in address 1
Write 64h in address 0
Write 93h in address 1
Counter B control mode setting
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 0 0 0
Automatic clear after error stop is disabled.
Automatic clear after normal stop is disabled.
CLR output control mode setting
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 0 0 0
Automatic clear after error stop is disabled.
Automatic clear after normal stop is disabled.
Comparator control mode setting
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1 0 0 1 1
P input is set to a comparator registor.
Q input is set to counter C.
Absolute value comparison is set.
CMP output is set to P>Q.

10-3 Parameter Setting

Among the parameter setting registers, the output pulse count setting register (R_1), the deceleration start point setting register (R_2), and the linear interpolation base setting register (R_8) should be set immediately before writing the drive command. This section describes the frequency multiplication ratio setting register (R_0), the startup frequency setting register (R_3), the maximum frequency setting register (R_4), the acceleration rate setting register (R_5), the deceleration rate setting register (R_6), and the S-shaped acceleration/deceleration section setting register (R_7). These registers must be set at least once after the power ON resetting, but the parameters that have not changed since then need not be set again. Also, the S-shaped acceleration/deceleration section setting register (R_7) need not be set when the S-shaped acceleration/deceleration are not used.

Figure 10-3: Parameter Setting Flow Chart (for Axis #1)



Write 04h in address 0

Maximum frequency setting

Set value 2134h = 8,500

Maximum frequency $V = \frac{16,384,000 \times 8,500}{65,536 \times 250} = 8,500$ **pps**

Write 34h in address 1

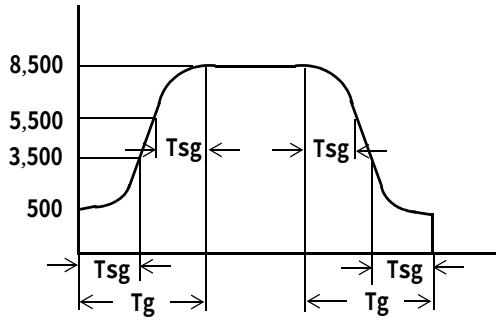
Write 21h in address 2

Write 07h in address 0

S-shaped acceleration/deceleration section setting

Set value 0BB8h = 3,000

The speed varies as shown in the following diagram.



Write B8h in address 1

Write 0Bh in address 2

Write 05h in address 0

Acceleration rate setting

Set value 00A0h = 160

Acceleration rate $g = \frac{16,384,000 \times 1 \times 160}{131,072} = 20,000$ **pps/s**

Write A0h in address 1

Acceleration time (linear) $Tg = \frac{131,072 \times (8,500 - 500)}{16,384,000 \times 160} = 0.4$ **s**

Acceleration time (S-shaped parabolic) $Tg = \frac{131,072 \times (8,500 - 500 + 2 \times 3,000)}{16,384,000 \times 160} = 0.7$ **s**

Write 00h in address 2

Acceleration time (S-shaped sine)

$$Tg = \frac{131,072 \times (8,500 - 500 - 2 \times 3,000 + \pi \times 3,000)}{16,384,000 \times 160} = 0.57 \text{ s}$$

Deceleration rate setting

Set value 00A0h = 160

Deceleration rate $g = \frac{16,384,000 \times 1 \times 160}{131,072} = 20,000$ **pps/s**

Deceleration time (linear) $Tg = \frac{131,072 \times (8,500 - 500)}{16,384,000 \times 160} = 0.4$ **s**

Deceleration time (S-shape) $Tg = \frac{131,072 \times (8,500 - 500 + 2 \times 3,000)}{16,384,000 \times 160} = 0.7$ **s**

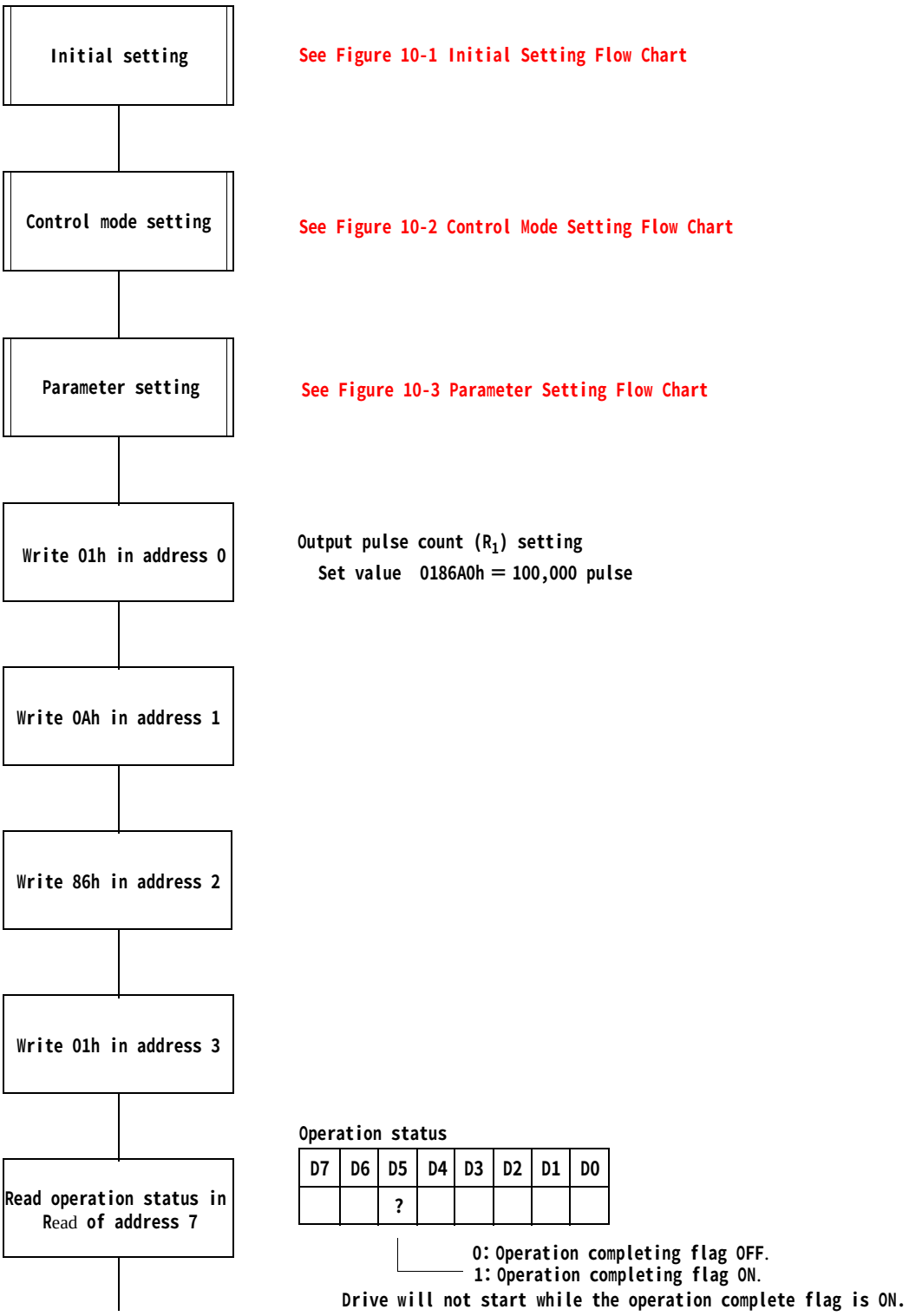
Acceleration time (S-shaped sine)

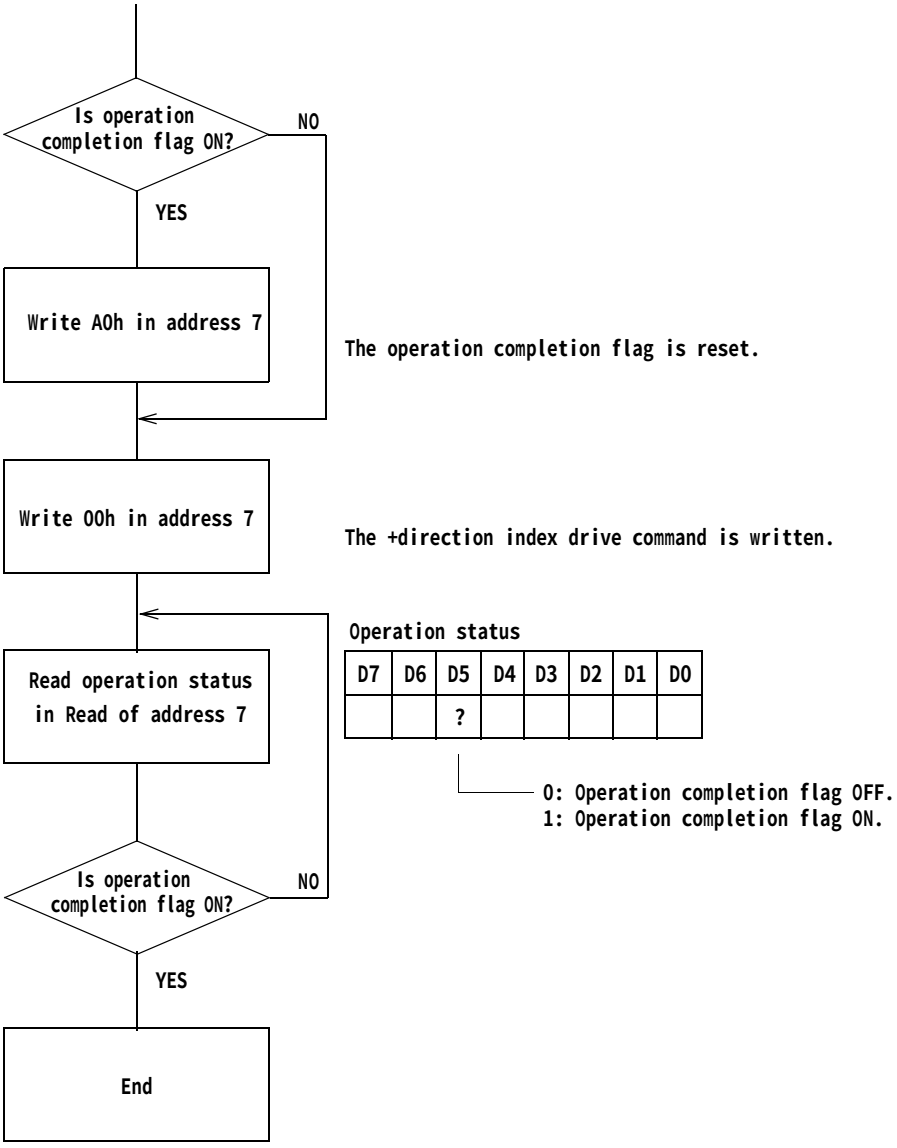
$$Tg = \frac{131,072 \times (8,500 - 500 - 2 \times 3,000 + \pi \times 3,000)}{16,384,000 \times 160} = 0.57 \text{ s}$$

10-4 Index Drive

This section takes the index drive of an independent axis as an example. As the drive is performed in the S-shaped acceleration/deceleration and deceleration start point automatic calculation modes, the acceleration rate (R_5) and deceleration rate (R_6) should be set to identical values. The end of operation is confirmed by polling the status.

Figure 10-4: Index Drive Flow Chart (for Axis #1)




Is operation completion flag ON?
NO
YES
Write A0h in address 7
The operation completion flag is reset.
Write 00h in address 7
The +direction index drive command is written.
Read operation status in Read of address 7
Operation status
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Operation completion flag OFF.
1: Operation completion flag ON.
Is operation completion flag ON?
NO
YES
End

10-5 Return-to-Origin Operation

While there are a large number of patterns for the return-to-origin sequence, the description in this section will take the following sequence and condition as an example. Figure 10-6 Index Drive Flow Chart (for Axis #1) shows the flow after the initial setting and parameter setting have completed.

Figure 10-5: Index Drive Flow Chart

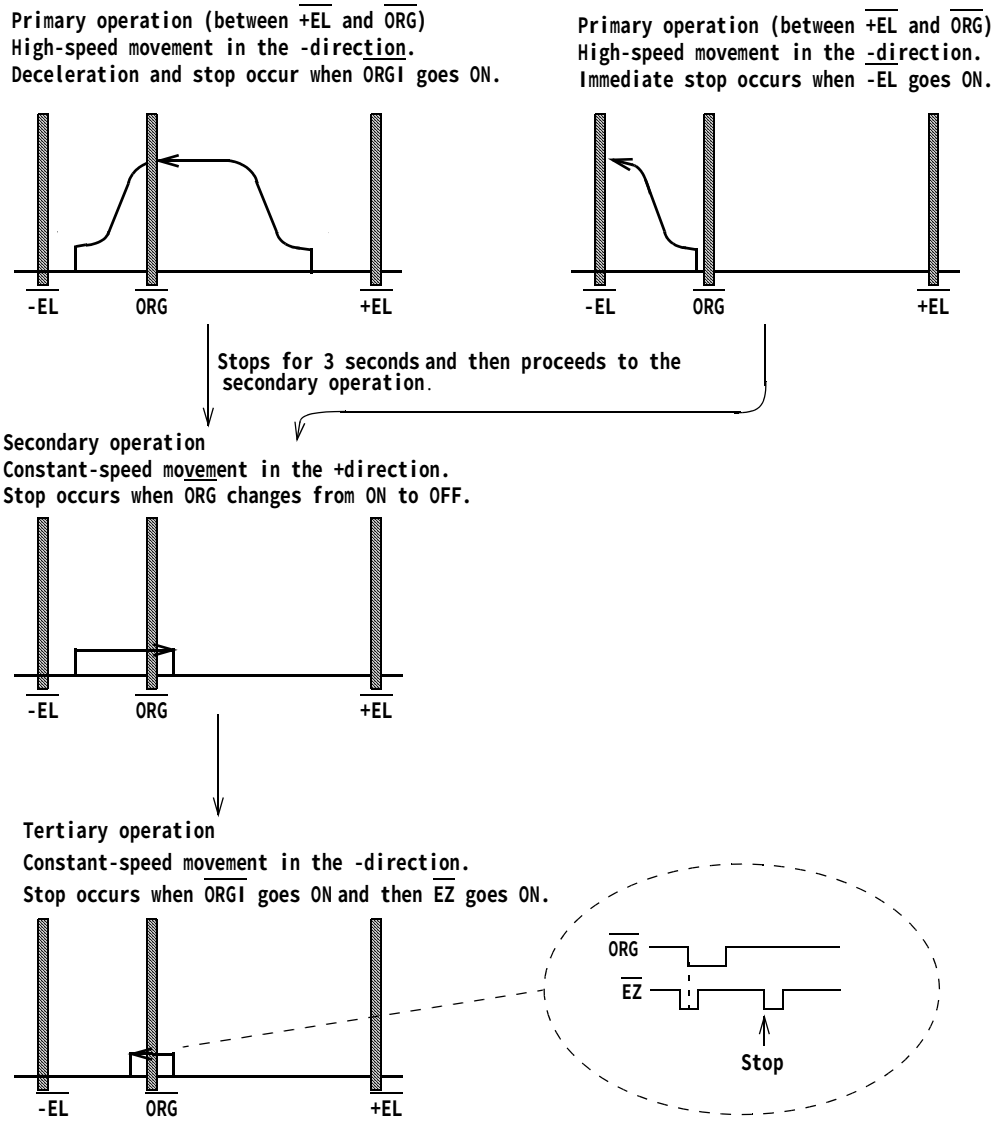
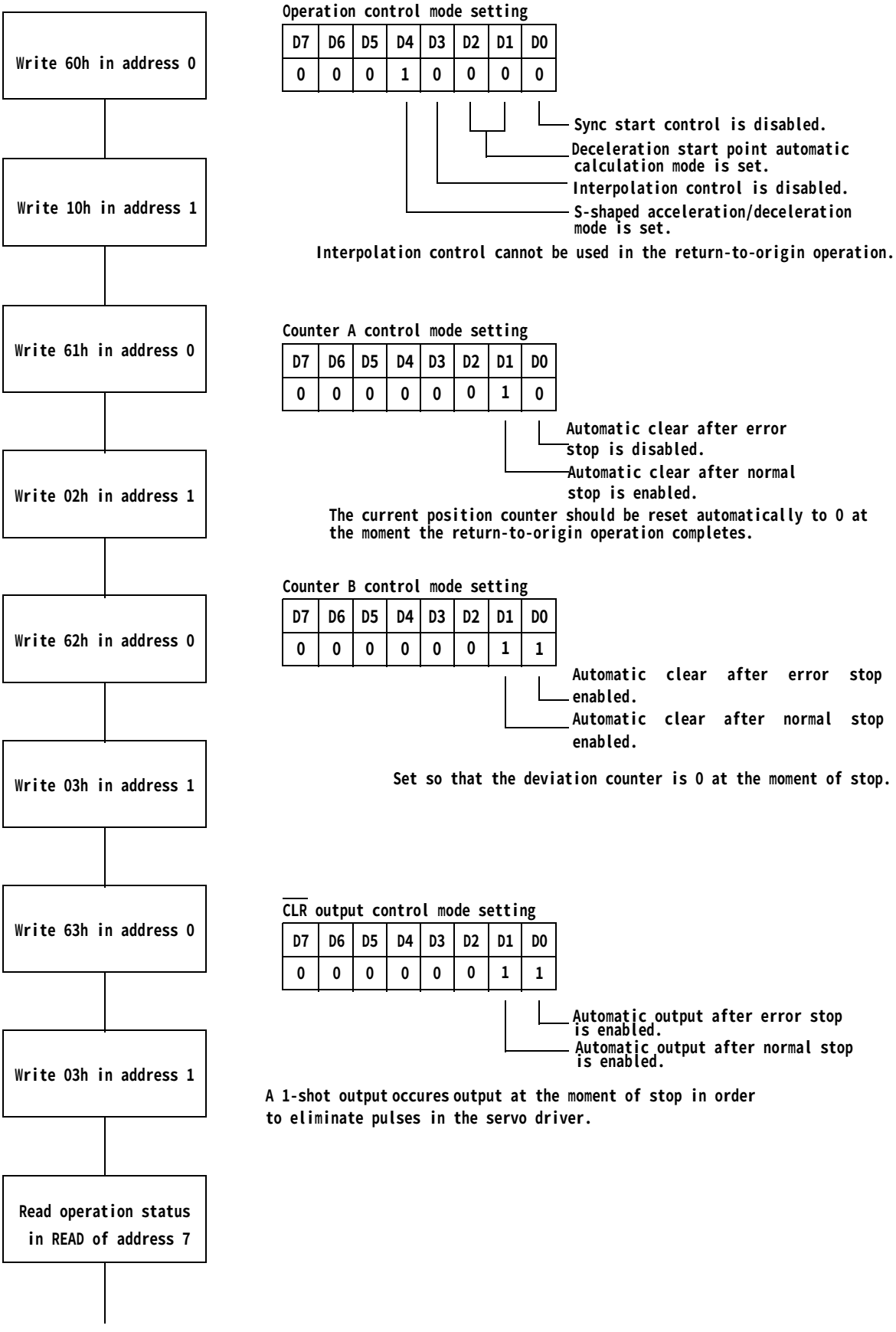
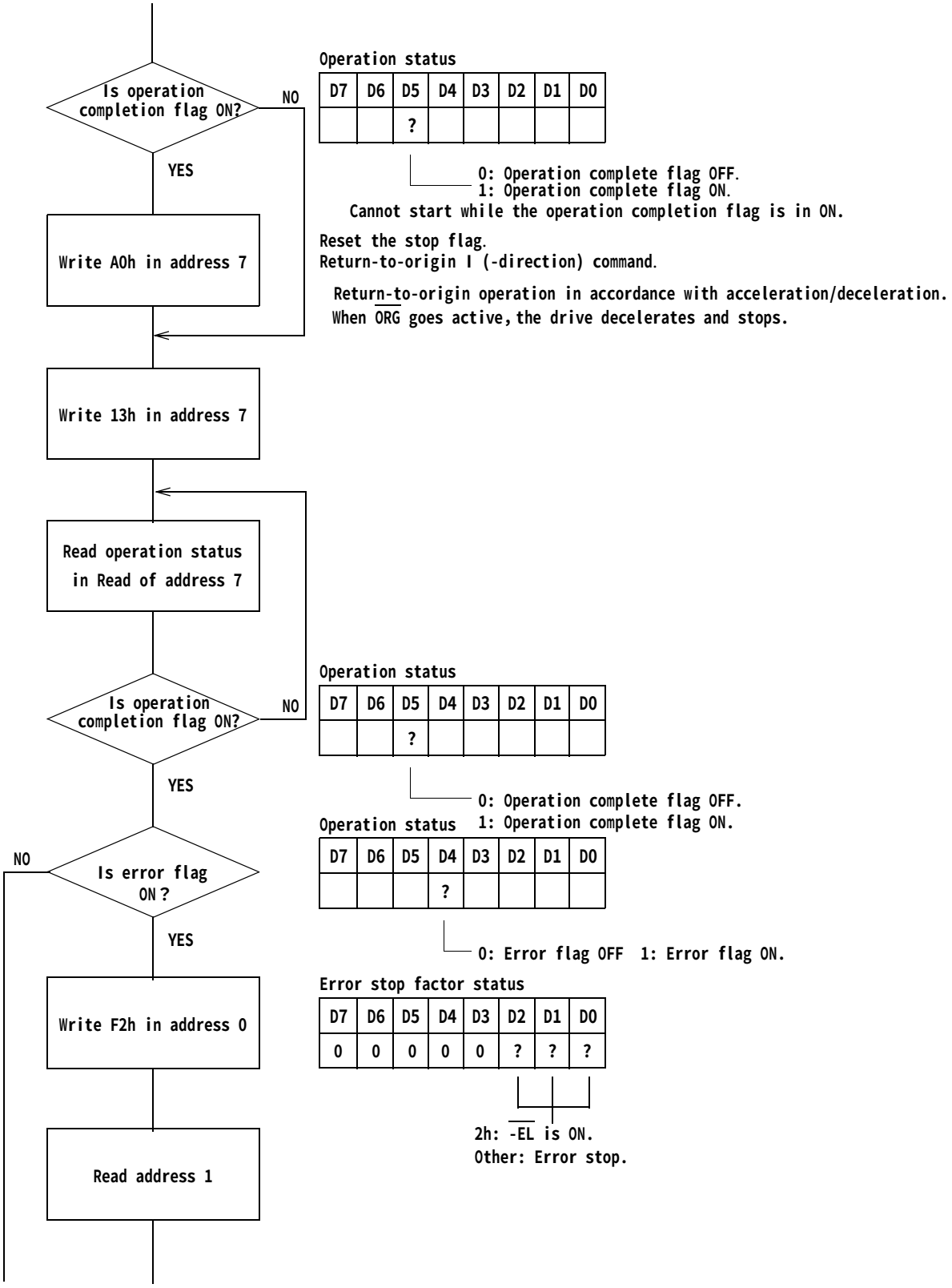
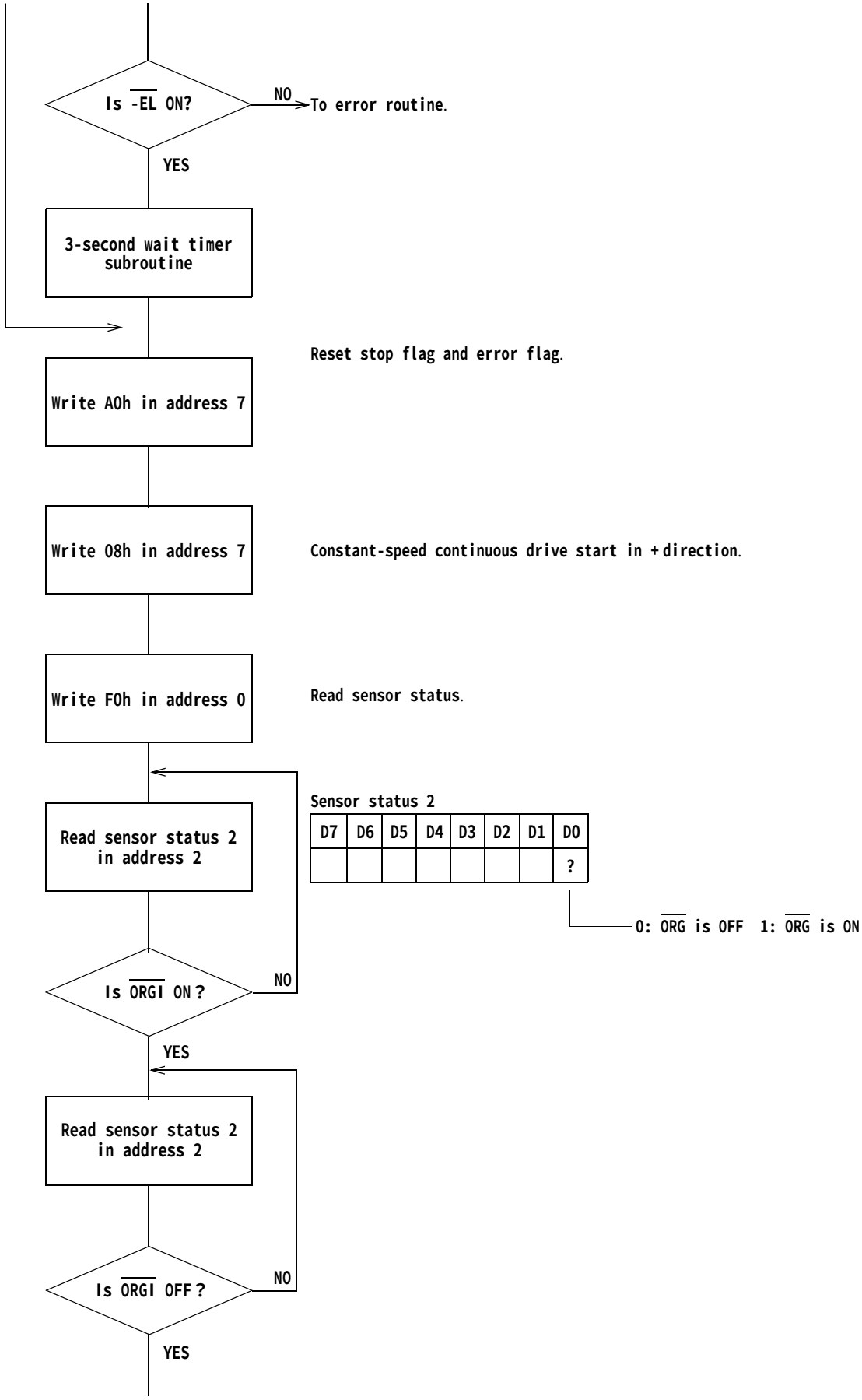
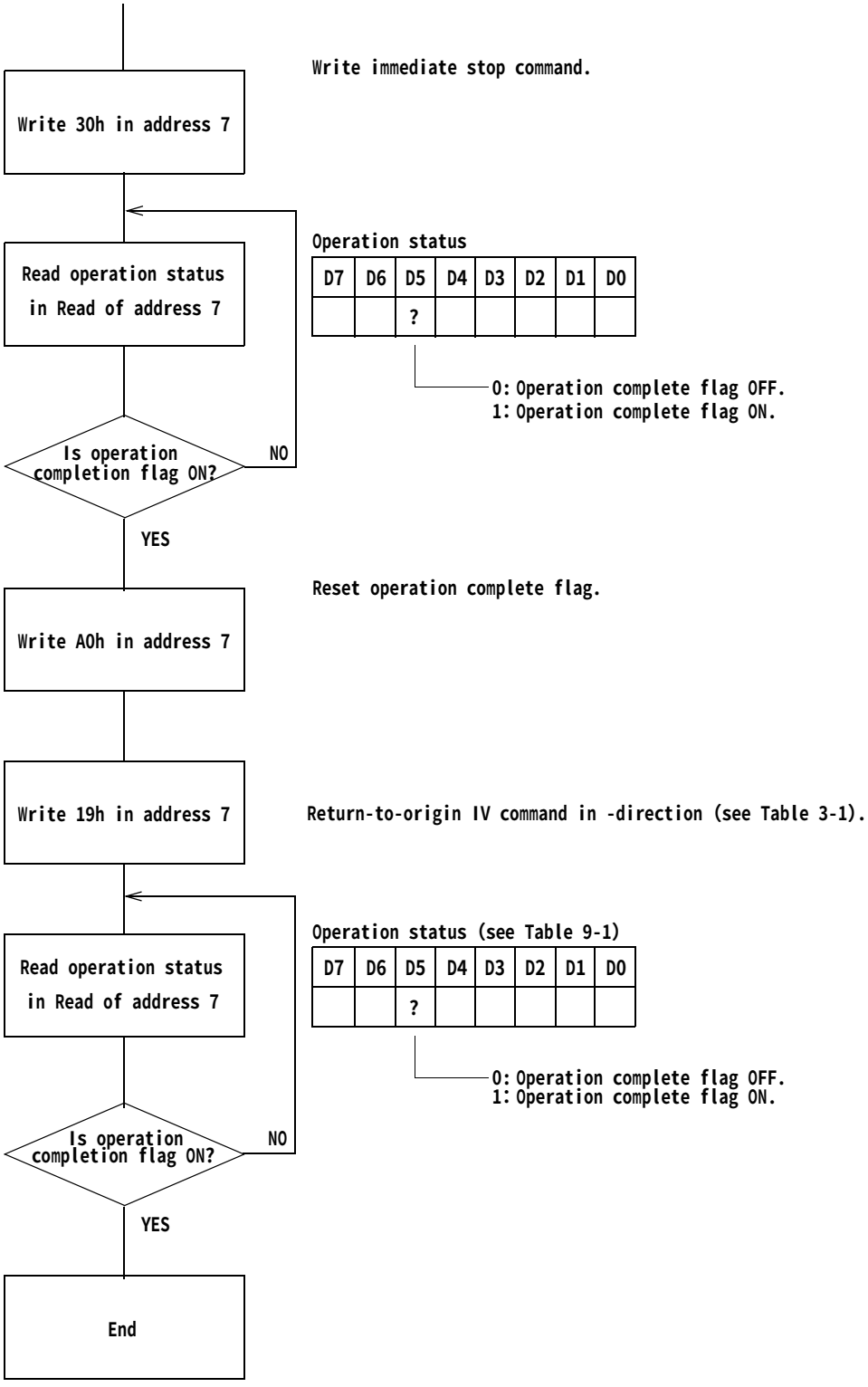


Figure 10-6: Index Drive Flow Chart (for Axis #1)




Is operation completion flag ON?
NO
YES
Write A0h in address 7
Write 13h in address 7
Read operation status in Read of address 7
Is operation completion flag ON?
NO
YES
Is error flag ON ?
NO
YES
Write F2h in address 0
Read address 1
Operation status
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Operation complete flag OFF.
1: Operation complete flag ON.
Cannot start while the operation completion flag is in ON.
Reset the stop flag.
Return-to-origin I (-direction) command.
Return-to-origin operation in accordance with acceleration/deceleration.
When ORG goes active, the drive decelerates and stops.
Operation status
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Operation complete flag OFF.
1: Operation complete flag ON.
Operation status
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Error flag OFF 1: Error flag ON.
Error stop factor status
D7 D6 D5 D4 D3 D2 D1 D0
0 0 0 0 0 ? ? ?
2h: -EL is ON.
Other: Error stop.


Is -EL ON?
NO
To error routine.
YES
3-second wait timer subroutine
Reset stop flag and error flag.
Write A0h in address 7
Write 08h in address 7
Constant-speed continuous drive start in + direction.
Write F0h in address 0
Read sensor status.
Sensor status 2
D7 D6 D5 D4 D3 D2 D1 D0
?
0: ORG is OFF 1: ORG is ON
Read sensor status 2 in address 2
Is ORGI ON ?
NO
YES
Read sensor status 2 in address 2
Is ORGI OFF ?
NO
YES


Write immediate stop command.
Write 30h in address 7
Read operation status in Read of address 7
Operation status
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Operation complete flag OFF.
1: Operation complete flag ON.
Is operation completion flag ON?
NO
YES
Reset operation complete flag.
Write A0h in address 7
Write 19h in address 7
Return-to-origin IV command in -direction (see Table 3-1).
Read operation status in Read of address 7
Operation status (see Table 9-1)
D7 D6 D5 D4 D3 D2 D1 D0
?
0: Operation complete flag OFF.
1: Operation complete flag ON.
Is operation completion flag ON?
NO
YES
End

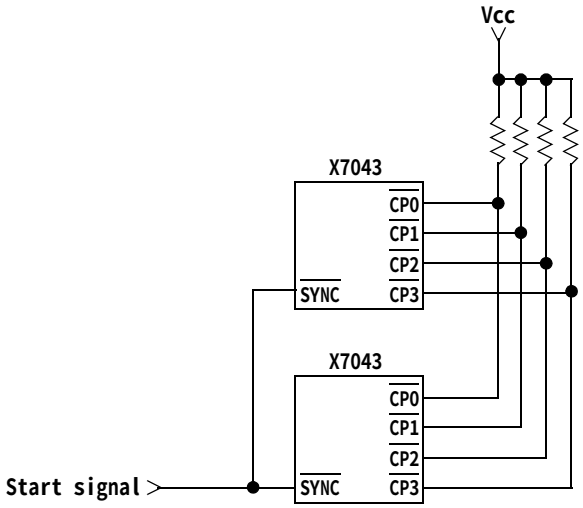
10-6 Linear Interpolation Drive

This LSI is capable of multi-axial linear interpolation between axes #1 to #4, but also between multiple chips. Make the connections shown in the following figure to perform linear interpolation between multiple chips. However, X7083 cannot perform linear interpolation between multiple chips.

10-6-1 Hardware Note

To perform linear interpolation using multiple numbers of this LSI, interconnect the $\overline{\text{SYNC}}$ and $\overline{\text{CP0}}$ to 3 terminals as shown in Figure 10-7.

Figure 10-7: Linear Interpolation Connection Scheme

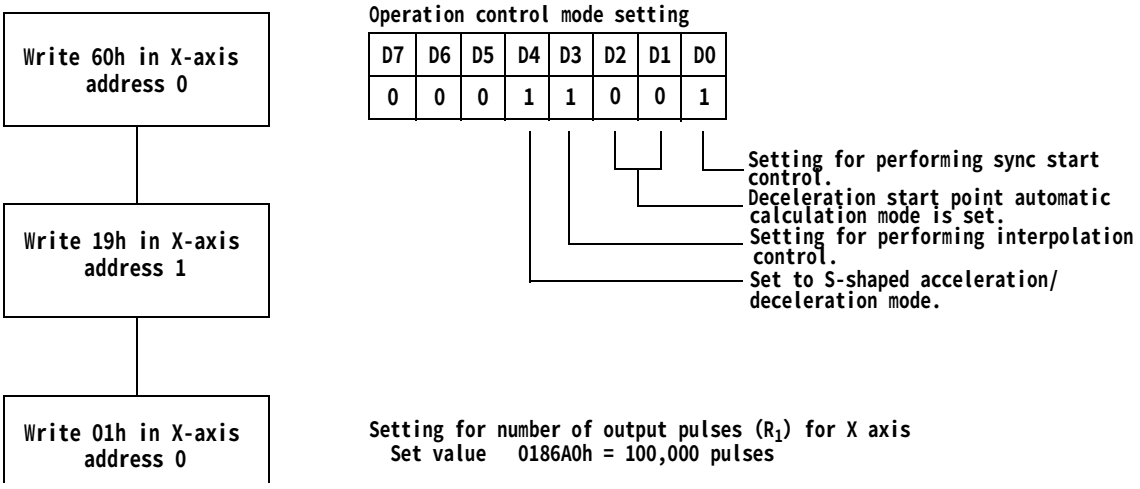


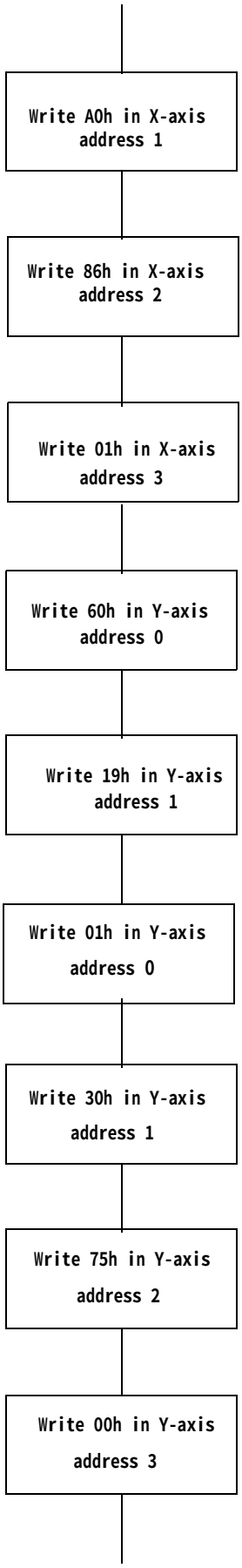
10-6-2 Flow of Linear Interpolation Drive

To drive multiple axes with linear interpolation, the frequency multiplication ratio (R_0), startup frequency (R_3), maximum frequency (R_4), acceleration rate (R_5), deceleration rate (R_6), and S-shaped acceleration/deceleration section (R7) parameter registers of all axes should be set to identical settings. The output pulse count registers (R_1) should be set to the respective movement amounts (pulse counts) of the axes, and the linear interpolation base setting register (R_8) should be set to the output pulse count of each axis at the maximum movement amount (pulse count) for all axes. In the deceleration start point manual setting mode, the deceleration start point registers (R_2) should be set for all axes at the value calculated based on the axis with the largest movement amount.

The following figure shows the flow chart after the initial setting and parameter settings.

Figure 10-8: Linear Interpolation Drive Flow Chart (for X and Y Axes)



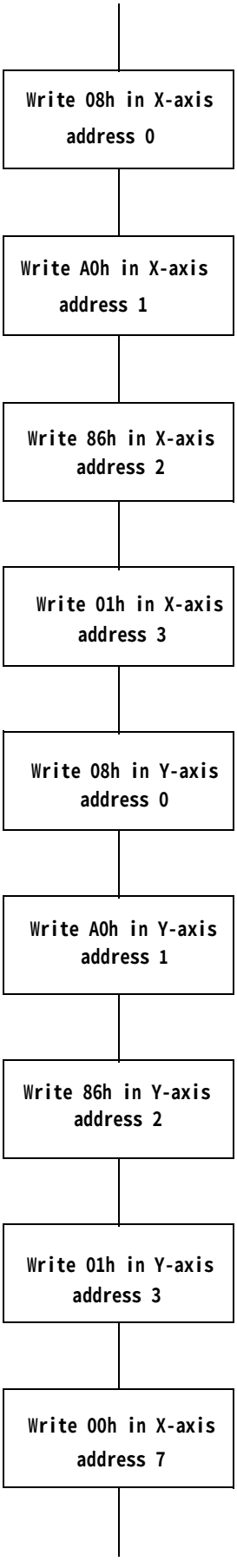


Operation control mode setting

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	0	0	1

- D0 = 1: Setting for performing sync start control.
- D1 = 0: Deceleration start point automatic calculation mode is set.
- D2 = 0: Setting for performing interpolation control.
- D3 = 1: Set to S-shaped acceleration/ deceleration mode.

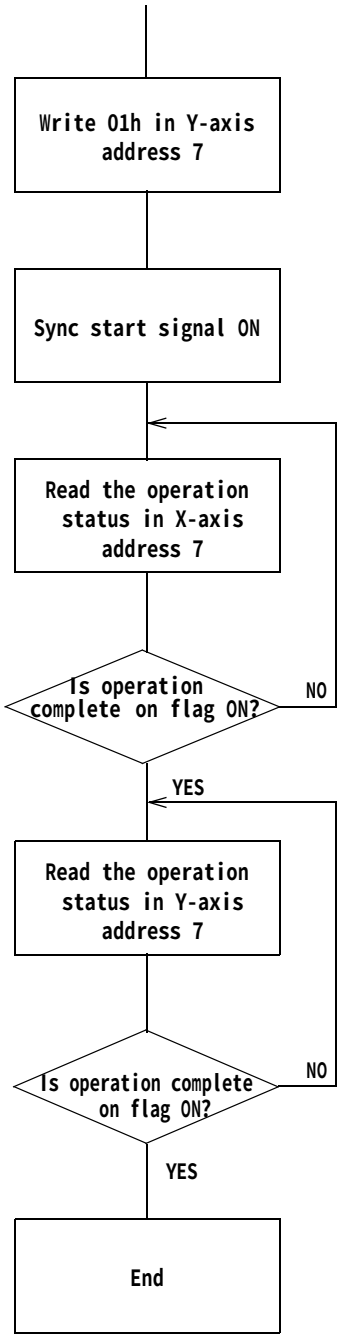
Setting for the number of output pulses (R_1)
Set value 007530h = 30,000 pulses



Setting for linear interpolation base (R_8)for X axis
Number of X-axis output pulses > number of Y-axis output pulses
Set value 0186A0h = 100,000

Setting for linear interpolation base (R_8)for Y axis
Number of X-axis output pulses > number of Y-axis output pulses
Set value 0186A0h = 100,000

When X axis is +direction pulse output



When Y axis is -direction pulse output

Operation status (See Table 9-1)

D7	D6	D5	D4	D3	D2	D1	D0
		?					

0: Operation complete flag OFF.
1: Operation complete flag ON.

11. Electrical Characteristics

11-1 Absolute Maximum Rating (Vss = 0V)

Item	Symbol	Rating	Unit
Supply voltage	$V_{dd}INT$	-0.3 to +4.6	V
	$V_{dd}IO$	-0.5 to +6.5	
Input voltage	V_{IN}	$V_{dd}IO$ = 3.3 V -0.3 to $V_{dd}IO$ + 0.3	V
		$V_{dd}IO$ = 5V -0.5 to $V_{dd}IO$ + 0.5	
Input current	I_{IN}	± 10	mA
Output current	I_O	± 25	mA
Storage temperature	T_{stg}	-65 to +150	℃

11-2 Recommended Operating Condition (Vss = 0V)

Item	Symbol	Rating	Unit
Supply voltage	$V_{dd}INT$	3.0 to 3.6	V
	$V_{dd}IO$	4.5 to 5.5 or 3.15 to 3.45	
Ambient temperature	T_a	0 to +70	℃

11-3 DC Characteristics

11-3-1 DC Characteristics (VddIO = 5V ± 10%, Ta = 0 to +70 ℃)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}		4.0			V
Low-level input voltage	V_{IL}				0.8	V
High-level input current	I_{IH}	V_{IH} = Vdd			10	μA
Low-level input current	I_{IL}		-10		10	μA
		V_{IL} = Vss	-200		-10	
High-level output voltage	V_{OH}	I_{OH} = -8mA	3.7			V
		I_{OH} = -100 μA	Vdd-0.2			
Low-level output voltage	V_{OL}	I_{OL} = 8mA			0.4	V
		I_{OL} = 100 μA			0.2	
Output leak current	I_{OZ}	V_{OUT} = Vdd or Vss	-10		10	μA
Hysteresis voltage *1	V_H		0.2	0.3		V

***1** $\overline{\text{INP}}$, $\overline{\text{ALM}}$, $\overline{\text{+EL}}$, $\overline{\text{-EL}}$, $\overline{\text{+SLD}}$, $\overline{\text{-SLD}}$, $\overline{\text{ORG}}$, $\overline{\text{EZ}}$, **IN0 to 7**, $\overline{\text{CLRA}}$, $\overline{\text{EA}}$, $\overline{\text{EB}}$, $\overline{\text{SYNC}}$, $\overline{\text{MARK}}$, $\overline{\text{CLK}}$, $\overline{\text{RST}}$, **A0 to 4,** $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$

11-3-2 DC Characteristics (VddIO = 3.3 V ± 10%, Ta = 0 to +70 ℃)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}		2.0			V
High-level input voltage*1			0.7 VddIO			
Low-level input voltage	V_{IL}				0.8	V
Low-level input voltage*1					0.3 VddIO	
High-level input current	I_{IH}	V_{IH} =Vdd			1	μA
Low-level input current	I_{IL}		-1			μA
		V_{IL} = Vss	-200		-10	
High-level output voltage	V_{OH}	I_{OH} = -8mA	2.4			V
High-level output voltage*1		I_{OH} = -4mA				
Low-level output voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Low-level output voltage*1		I_{OL} = 4mA				
Output leak current	I_{OZ}	V_{OUT} = Vdd or Vss	-1		1	μA
Hysteresis voltage *2	V_H		0.1	0.4		V
Static current consumption	I_{DDS}	V_{IN} = Vdd or Vss			60	μA

***1 $\overline{\text{CP0 to 3}}$**

***2 $\overline{\text{INP}}$, $\overline{\text{ALM}}$, $\overline{\text{+EL}}$, $\overline{\text{-EL}}$, $\overline{\text{+SLD}}$, $\overline{\text{-SLD}}$, ORG, $\overline{\text{EZ}}$, IN0 to 7, $\overline{\text{CLRA}}$, $\overline{\text{EA}}$, $\overline{\text{EB}}$, $\overline{\text{SYNC}}$, $\overline{\text{MARK}}$, $\overline{\text{CLK}}$, $\overline{\text{RST}}$, A0 to 4, $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$**

11-4 Switching Characteristics

11-4-1 CPU Interface (VddIO = 5V ± 0.25 V, VddINT = 3.3V, Ta = 0 to +70 ℃)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}				20	MHz
Clock period	t_{CLK}		50			ns
Clock Low duration	t_{PWL}		8			ns
Clock High duration	t_{PWH}		25			ns
Read address stable time	t_{AR}		10			ns
Read address retention time	t_{RA}		2			ns
Read pulse width	t_{RR}		13			ns
Data delay time	t_{RD}	CL = 100pF			15	ns
Data float delay time	t_{DF}	CL = 100pF			15	ns
Write address stable time	t_{AW}		0			ns
Write address retention time	t_{WA}		0			ns
Write pulse width	t_{WW}		13			ns
Data setting time	t_{DW}		7			ns
Data retention time	t_{WD}		0			ns
Reset pulse width	t_{RST}		$3t_{CLK}$			ns
Reset operation time	t_{RSTM}				3_{tCLK}	ns

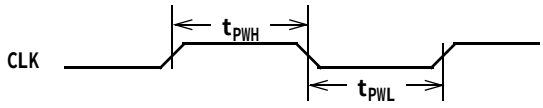
t_{CLK} : Reference clock period (Min. 50 ns)

11-4-2 CPU Interface (VddIO = 3.3V ± 0.15V, VddINT = 3.3V, Ta = 0 to +70 ℃)

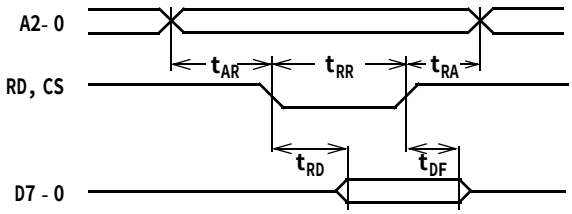
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}				20	MHz
Clock period	t_{CLK}		50			ns
Clock Low duration	t_{PWL}		12			ns
Clock High duration	t_{PWH}		21			ns
Read address stable time	t_{AR}		10			ns
Read address retention time	t_{RA}		0			ns
Read pulse width	t_{RR}		16			ns
Data delay time	t_{RD}	CL = 100 pF			20	ns
Data float delay time	t_{DF}	CL = 100 pF			19	ns
Write address stable time	t_{AW}		0			ns
Write address retention time	t_{WA}		0			ns
Write pulse width	t_{WW}		16			ns
Data setting time	t_{DW}		9			ns
Data retention time	t_{WD}		0			ns
Reset pulse width	t_{RST}		$3t_{CLK}$			ns
Reset operation time	t_{RSTM}				$3t_{CLK}$	ns

t_{CLK} : Reference clock period (Min. 50 ns)

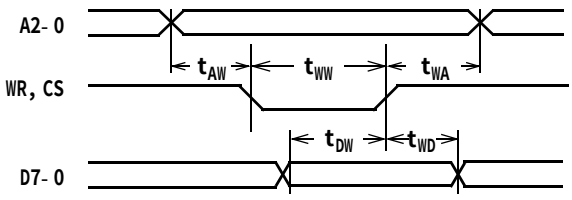
Clock



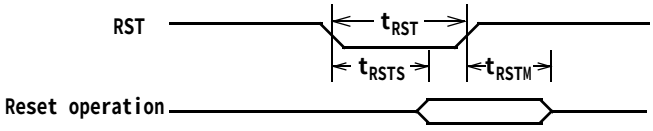
Read cycle



Write cycle



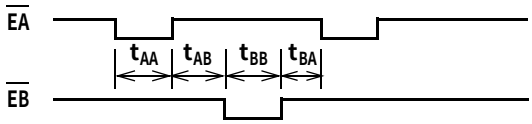
Reset cycle



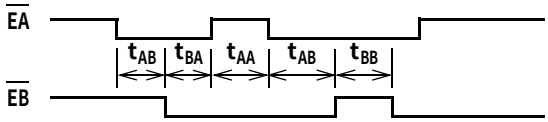
11-4-3 Encoder Interface

Item	Symbol	MIN.	TYP.	MAX.	Unit
Edge interval when phase B edge occurs after phase A edge	t_{AB}	$2.5t_{CLK}$			ns
Edge interval when phase A edge occurs after phase B edge	t_{BA}	$2.5t_{CLK}$			ns
Edge interval when phase A edge occurs after phase A edge	t_{AA}	$2.5t_{CLK}$			ns
Edge interval when phase B edge occurs after phase B edge	t_{BB}	$2.5t_{CLK}$			ns

2-clock inputs

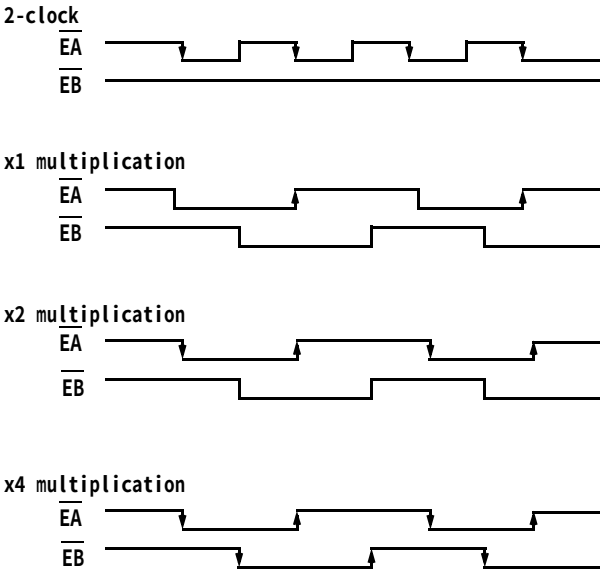


2-phase clock input

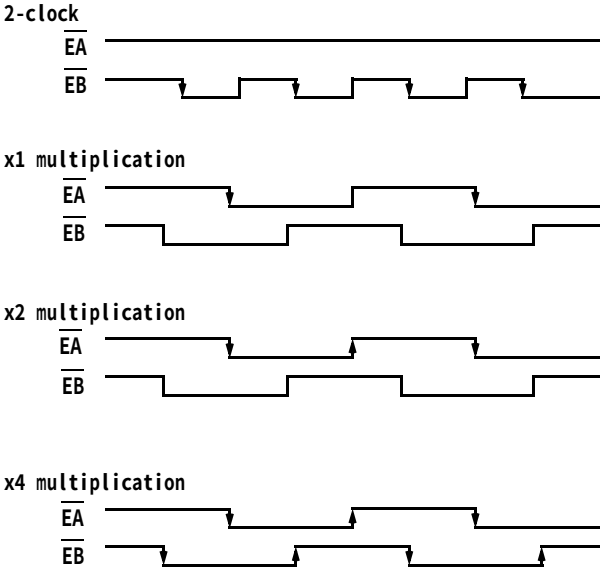


Encoder input count timing (when forward counting is set)

Upward counting



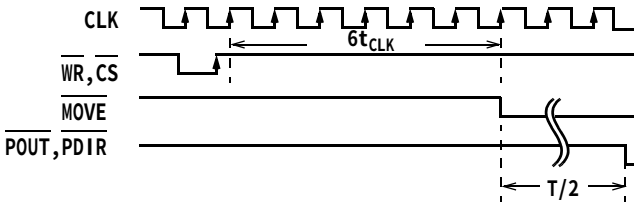
Downward counting



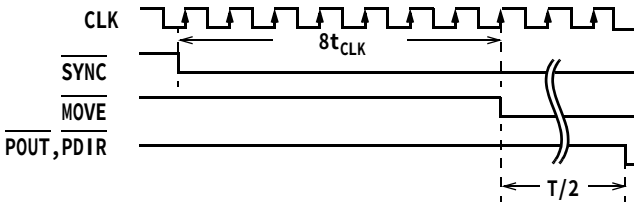
11-4-4 Input and Output Interface

Pulse output start

A sync start mode



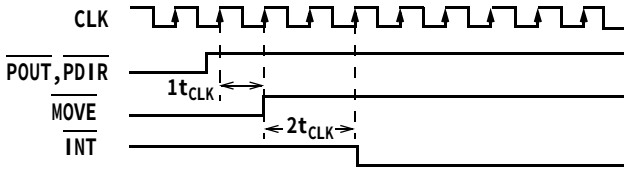
Sync start mode



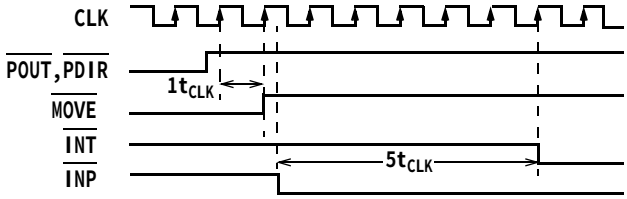
T: 1 period of startup frequency

Pulse stop

Setting for completing operation when the pulse output completes.



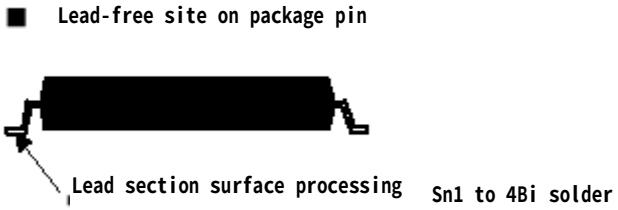
Setting of completing operation when the positioning has completed.

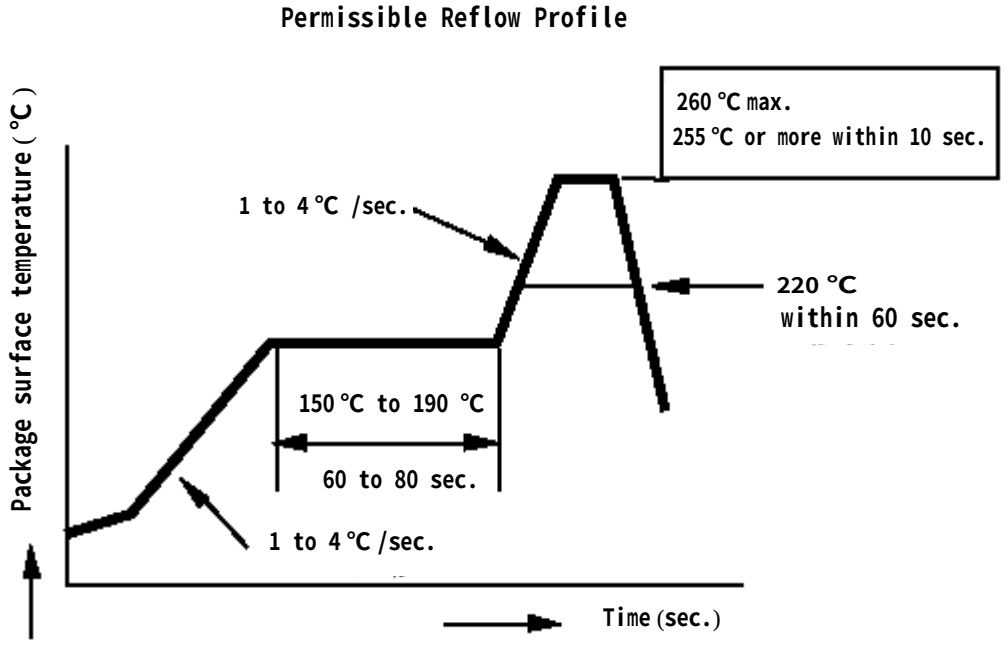


12. Lead-Free Specifications

Generally, reflow temperature increases when mounting components, using lead-free solder paste. Therefore, the package was designed to withstand a reflow temperature of 260 ℃ (max.). In addition, reflow is supported up to twice.

Figure 12-1: Lead-Free Specification





This User's Manual describes information as of April 2005. To improve this product, its specifications are subject to change without notice.